

LQ-1500

SERVICE MANUAL

EPSON[®]



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INTRODUCTION

This technical manual describes the principle of mechanical and electrical operations, as well as the maintenance and repair procedures, of the EPSON LO-1500 Dot Matrix Printer.

Chapters 4 through 6 of the manual deal with the fundamental troubleshooting, maintenance and repair of the LO-1500.

For detail on the disassembly, assembly, troubleshooting and maintenance of the Model-3660 Printer Mechanism, refer to the separately published "Technical Manual of EPSON Model-3660".

* The contents of this manual are subject to change without notice

CHAPTER 1 GENERAL

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1 .1 Product Overview

The LO-1500 is a serial terminal printer, featuring 200 CPS, bi-directional printing (draft pica mode) with logical seeking capability, and 24 x 24 dot-matrix character formation. All interfaces for the LO-1500 which permit connection of the printer to various computers are optional. The interface circuit boards are cartridge type, which can be set snugly into the housing.

Should maintenance or repair be required, the printer mechanism and circuit boards of the LQ-1500 are readily replaceable. The technician can perform maintenance and repair quite easily by referring to this manual.

1.2 LQ-1500 Interface Overview

(1) Centronics-compatible, parallel interface

This standard communication link permits data exchange with many computers without modification or addition of other peripheral devices.

(2) RS-232C/Current Loop Serial Interface

A 20 mA current loop type, serial interface which permits the printer to receive data at a bit rate ranging from 75 to 19200 BPS.

(3) IEEE-488 Interface

An optional interface which permits parallel communication between the printer and any computer or measuring instrument which is equipped with bus structure conforming the IEEE-488 Std. 488-1975.

1.3 General Specifications

(1) Printing Method Impact dot matrix

(2) Character 1. Draft
 2. Near letter quality (LO)
 3. Proportional (standard)
 4. Multi-font (with option card)
 5. Super/subscript in each above character style. (1 to 4.)

(3) Character Structure

Character	Normal	Super/Subscript
Draft	9 x 17 font	7 x 11 font
LO	15 x 17 font	11 x 11 font
Proportional	37 x 17 font	23 x 11 font

(4) Character Size See Table 1. on the page 1-3

(5) Column Width See Table 1. on the page 1 - 3.

(6) Print Speed See Table 1. on the page 1 - 3.

(7) Paper Feed Friction feed (standard)
 Adjustable tractor feed (option)

(8) Paper

① Cut sheet

Paper width 182 mm to 364 mm

Paper thickness 0.06 mm to 0.1 mm

Weighing 45 kg to 70 kg (52 to 82 g/m*)

② Fanfold paper

p a p e r w i d t h 101 mm to 406 mm

C o p i e s 4 sheets max. (include original)

Paper thickness and Weight

The Number of Sheets	Weighing	Paper Thickness	Setting of the Head Adjusting Lever
1	45 to 70 kg (52 to 82 g/m ²)	0.06 to 0.1 mm	2nd step
2	30 to 35 kg (35 to 40 g/m ²)	0.1 mm	2nd step
3	30 to 35 kg (35 to 40 g/m ²)	0.15 m	3rd step
4	30 to 35 kg (35 to 40 g/m ²)	0.2 mm	4th step

Notes:

1. Jointing finish of copies should be point or line pasting.
2. Release the friction feed during the tractor feed operation.
3. Set the head adjusting lever as shown in above table.
However, adjust the step setting within range +1 step, depending on print density.

- (9) Paper Insertion Rear
- (1 0) Line Spacing 1/6", 1/8" or programmable
- (1 1) Print Direction..... Bidirectional printing with logical seeking.
In bit image and double-strike mode, unidirectional printing from left to right is selected when the power is ON.
Bidirectional printing is also possible using ESC U.
- (1 2) Line Feed Repeat Rate 120 ms/line (when 1/6" line feed is performed intermittently)
100 ms/line (when 1/6" line feed is performed continuously)
- (1 3) Ribbon.. Exclusive cartridge ribbon (Black)

Table 1

Print mode	*1 C.W.	*2 Char.W.	*3 D. D.	Printed Speed (CPS)		*4 Char. Size (mm)		*5 S/S Char. Size (mm)	
	(CPL)	(CPI)	(DPI)	Draft	LQ	Width	Height	Width	Height
Pica	136	10	120	200	67	2.1	2.5	1.7	1.7
Enlarged	68	5	120	100	33	4.2	2.5	3.4	1.7
Emphasized	136	10	120	100	67	2.3	2.5	1.9	1.7
Emphasized & Enlarged	68	5	120	50	33	4.6	2.5	3.8	1.7
Condensed	233	17	240	167	—	1.0	2.5	0.8	1.7
Condensed & Enlarged	116	8.6	240	83	—	2.0	2.5	1.7	1.7
Elite	163	12	180	162	80	1.4	2.5	1.7	1.7
Enlarged	81	6	180	81	40	2.8	2.5	3.4	1.7
Emphasized	163	12	180	81	80	1.6	2.5	1.9	1.7
Emphasized & Enlarged	81	6	180	40	40	3.2	2.5	3.8	1.7
Condensed	272	20	240	200	—	1.0	2.5	0.8	1.7
Condensed & Enlarged	136	10	240	100	—	2.0	2.5	1.7	1.7
Proportional	116	8.6	360	—	57	2.6	2.5	—	—
Enlarged	58	4.3	360	—	28	5.2	2.5	—	—
Emphasized	116	8.6	360	—	57	2.8	2.5	—	—
Emphasized & Enlarged	58	4.3	360	—	28	5.6	2.5	—	—
Proportional Super/Subscript	174	12.8	360	—	86	—	—	1.7	1.7
Enlarged	87	6.4	360	—	43	—	—	3.4	1.7
Emphasized	174	12.8	360	—	86	—	—	1.8	1.7
Emphasized & Enlarged	87	6.4	360	—	43	—	—	3.7	1.7

*1 C.W. = Column Width

*2 Char.W. = Character Width

*3 D.D. = Dot Density

*4 Char. Size = Character Size

*5 S/S Char. Size = Super/Subscript Character Size

Notes:

1. Above values for Proportional are calculated by width of the max. character "W".
2. DPI of LQ (except Proportional) is 180.

(14) Environment

Temperature	Operating	5°C to 35°C (41°F to 95°F)
	Storage	-30°C to 65°C
Humidity.....	Operating	10% to 80% (No condensation)
	Storage	5% to 85% (No condensation)
Resistance to impact.....	Operating	1G (1 msec. max.)
	Storage	2G (1 msec. max.)
Resistance to vibration.....	Operating	0.25G, 55 Hz (max.)
	Storage	0.5 G, 55 Hz (max.)
Insulation resistance	10 megohms between AC power line and chassis.	
Dielectric strength.....	AC 1KV (R.M.S.), 50 or 60 Hz for more than 1 minute between AC power line and chassis.	

(15) Electrical Requirement

Power supply	AC 90V to 132V (for U.S.A.)
	AC 198V to 264V (for Europe)
Frequency	49.5 to 60.5 Hz
Power consumption	300 VA max.
	60 VA typ.

(16) Reliability

MTBF.....	5 × 10 ⁶ lines (excluding head life expectancy)
Print head life expectancy.....	2 × 10 ⁸ strokes (at every dot wire on the print head)
Ribbon life expectancy	3 × 10 ⁶ characters (Draft)

(17) Physical Dimensions and Weight

Dimensions.....	130 (H) × 604 (W) × 363 (D) mm
	With tractor unit 183 (H) mm
	With cut sheet feeder 320 (H) mm
Weight.....	14 kg (including I/F Unit)

1.4 Major Components

The LQ-1500 consists, in a broad classification, of the following five major components

- (1) Housing
- (2) Model-3660 printer mechanism
- (3) Control circuit boards
- (4) Interface circuit boards
- (5) Power supply circuit boards

The housing of the LQ-1500 consists of an upper case and lower case. The lower case is designed to facilitate mounting of the following components.

Circuitry for the LQ-1500 is located on five different boards: the UXFIL and UXPS/PSU 24E boards which house the power supply; the UXMCL board, which contains most of the control circuitry; the UXDRV, which handles print mechanism drive circuitry, and a interface board (IUPIF or IURS or IUIE) which serves as computer interface.

(1) Housing (Fig. 1 .1)

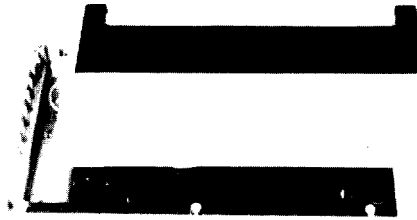


Fig 1 .1 Upper and lower cases

(2) Model-3660 printer mechanism (Fig. 1.2)

The mechanism is an assembly of all the mechanical components including two stepper motors, a print head, a ribbon feeding mechanism, a carriage assembly, sensors, and a frame section. One stepper motor operates the print head carriage, while the other works as the paper feed motor. The Model-3660 is designed to permit easy maintenance.

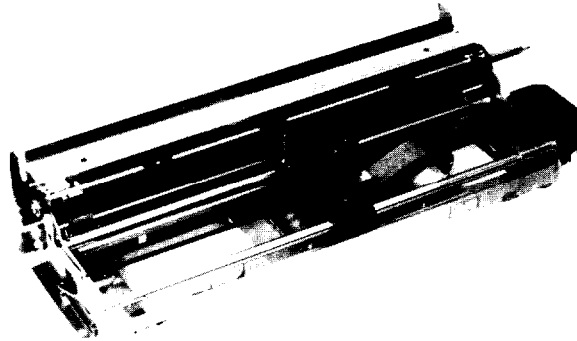


Fig. 1.2 Model-3660 printer mechanism

(3) Contrl circuit boards (Fig. 1.3)

The control circuit is distributed between two circuit boards, the UXMCL and UXDRV. The UXMCL circuit board performs the central processing, and the UXDRV circuit board drives the Model-3660 printer mechanism.

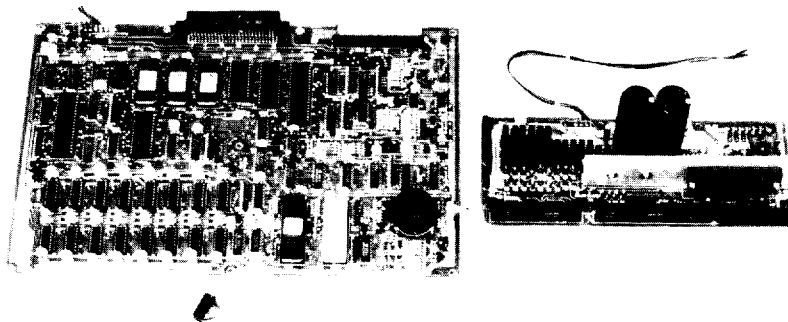


Fig. 1.3 Control circuit boards

(4) Interface circuit boards (Fig. 1.4)

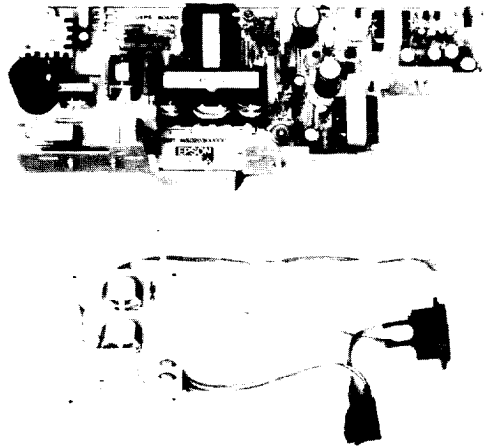
An interface circuit board exchanges data between the host computer and UXMCL circuit board.



Fig. 1.4 Interface circuit board

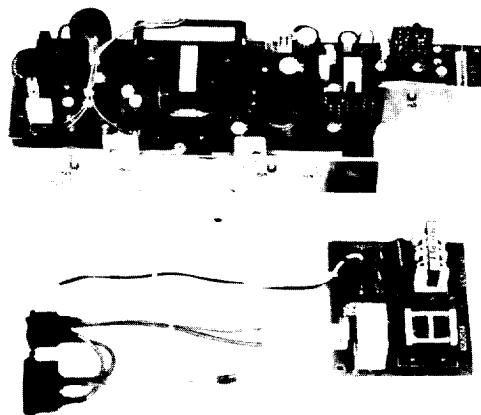
(5) Power supply circuit boards (Fig. 1.5)

The power supply circuit of the LQ-1500, consists of two major components, the UXFIL and UXPS/PSU 24E circuit boards. Both circuit boards are located in the rear righthand corner. The UXPS/PSU 24E circuit board supplies DC +24V, +12V, -12V and +5V to the control circuit and the interface circuit.



UXPS

Fig 1.5 Power supply circuit board (100/120V version)



PSU 24E

Fig 1.6 Power supply circuit board (220/240V version)

CHAPTER 2

PRINCIPLES OF OPERATION

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2.1 General

This chapter provides the description of signals at the various connectors electrically interconnecting such major components as printer mechanism, control circuits, interface circuit, power supply circuit, and control panel of EPSON LO-1500 Terminal Printer, and explains the operating principles of the various mechanism around the electric circuit of the printer.

2.2 Connection Diagram (Fig. 2.1)

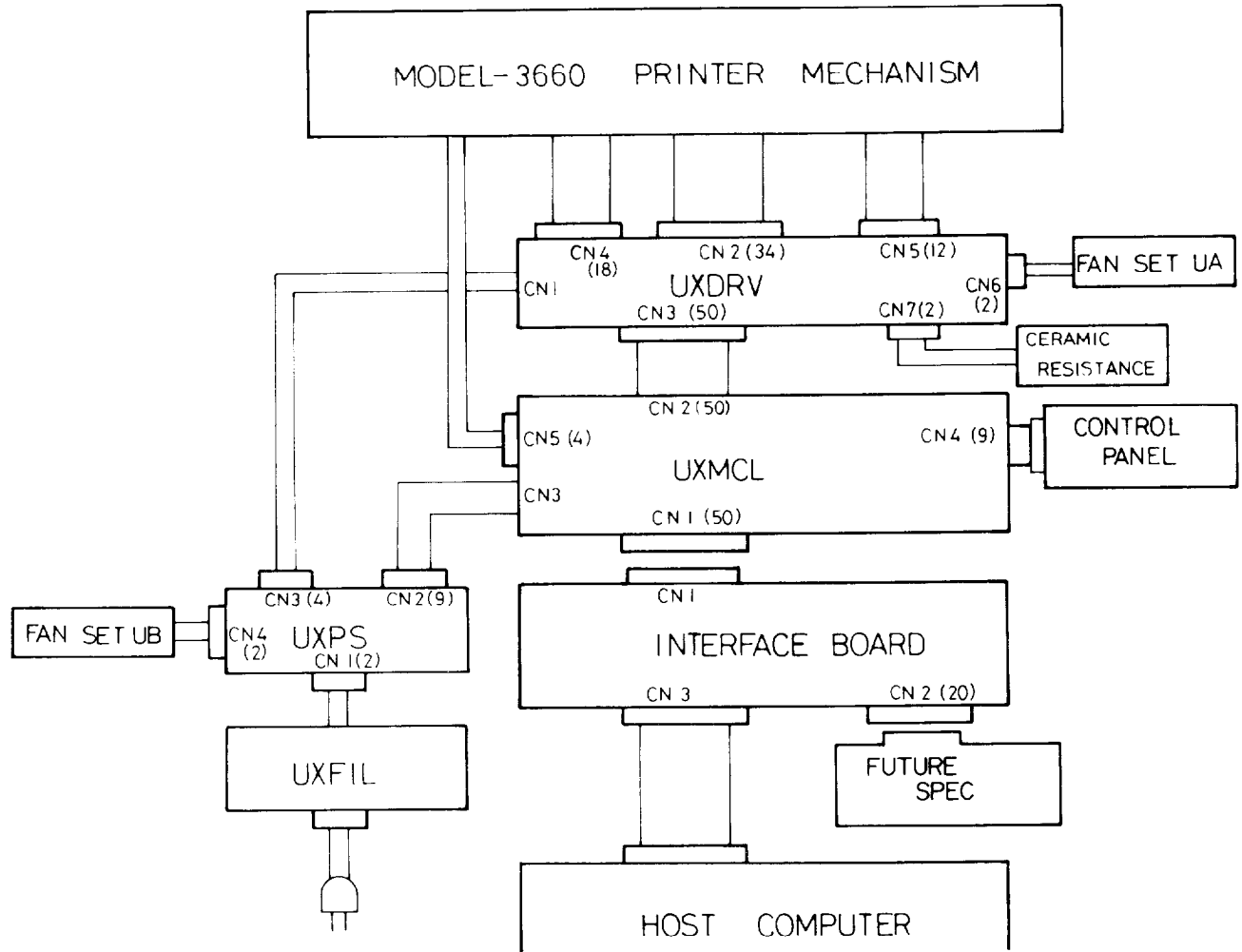


Fig. 2.1 Connection diagram

The CPU Z-80A provides overall control of the LQ-1500. In addition the LQ-1500 is supported by two slave CPUs: the 8042(8742), which controls the carriage motor; the 8041(8741), which controls the paper feed motor.

Other major LSIs include:

- 8255AC5 Output port for head pin drive data
- 8259A Interrupt controller
- 8253-5** **Timer counter**
- 2764(231 28) ROM which stores control programs and character patterns
- uPD41 6-3 RAM which is used as the input data and print data buffer
- uPB6101 -009 Gate array which controls LSIs by receiving control signals from CPU Z-80A

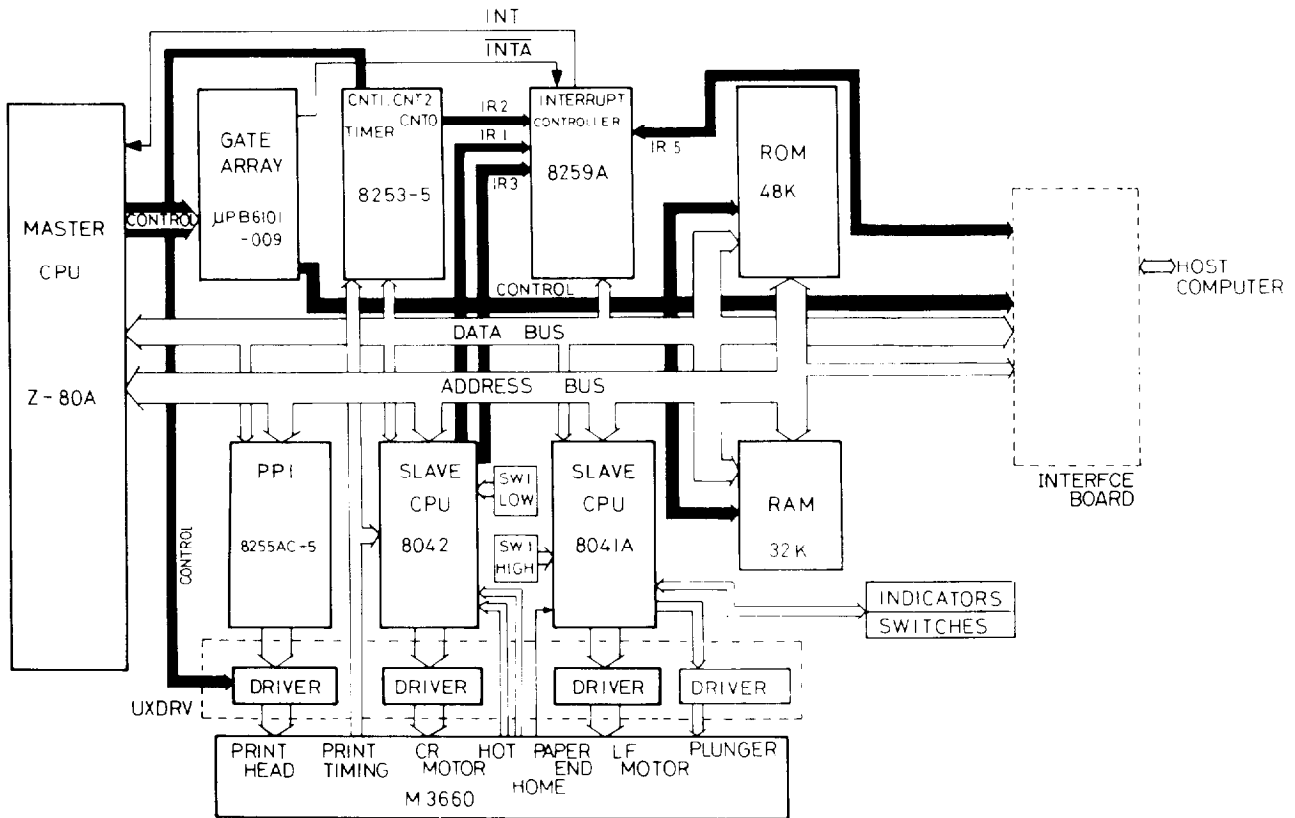


Fig. 2.2 Block diagram

2.3 Connector Pin Assignment

2.3.1 Connector on UXMCL circuit board

1) Table 2.1 CN1 pin assignment

- (a) Use Used for data exchange between the main circuit board and the interface circuit board
- (b) Number of pins 50

Table 2.1 Pin assignment (CN1 of UXMCL)

Signal Pin No.	Signal	Direction	Description
1	GND		Logic ground
2	GND		Logic ground
3	V _x	OUT	The SLCT signal is made HIGH at +5V power on.
4	PE	OUT	DC level signal to indicate the end of paper. Low = Normal operating condition. High = Paper supply depleted.
5	RST IN	IN	High = Normal operating condition, the pulse width must be more than 50 μ s at the receiving terminal. Low = Reset printer is initialized. Print buffer is cleared.
6	ERR	OUT	This signal becomes LOW when the printer is in the following conditions: 1. PAPER END state (sensed at line feed) 2. OFF-LINE state 3. Print failure due to other abnormal condition * The PAPER END state is sensed at line feed. * If DIP SW2-2 on the interface circuit board is turned on or ESC8 has been input to the printer, the ERROR signal does not become LOW even in the PE condition.
7	GND		
8	IBUSY	IN	Low = Input buffer is not full. High = Input buffer is full. The signal is used to turn on the READY lamp of the indicator.
9	EXTPRG	OUT	External program selection signal (Not used at the moment)
10	MRD	OUT	Memory read signal LOW output is made when BUSACK = High at MRQ, RD. However, it is not output in the INTACK cycle.
11	ICSCG	OUT	External character selection signal (Not used at the moment)
12	ICSPRG	OUT	External program selection signal (Not used at the moment)
13	A12	OUT	Address bit 12
14	A13	OUT	Address bit 13
15	A10	OUT	Address bit 10
16	A11	OUT	Address bit 11
17	A8	OUT	Address bit 8
18	A9	OUT	Address bit 9
19	A6	OUT	Address bit 6
20	A7	OUT	Address bit 7

Signal Pin No.	Signal	Direction	Description
21	A4	OUT	Address bit 4
22	A5	OUT	Address bit 5
23	A2	OUT	Address bit 2
24	A3	OUT	Address bit 3
25	A0	OUT	Address bit 0
26	A1	OUT	Address bit 1
27	GND		Logic ground
28	GND		Logic ground
29	D6	IN/OUT	Data bit 6
30	D7	IN/OUT	Data bit 7
31	D4	IN/OUT	Data bit 4
32	D5	IN/OUT	Data bit 5
33	D2	IN/OUT	Data bit 2
34	D3	IN/OUT	Data bit 3
35	D0	IN/OUT	Data bit 0
36	D1	IN/OUT	Data bit 1
37	GND		Logic ground
38	GND		Logic ground
39	IR4	IN	Interrupt request signal, priority 4
40	IR5	IN	Interrupt request signal, priority 5
41	ICS7	OUT	Chip select signal of I/O port 8255 AC-5 on the interface circuit board. * This signal is LOW when 8255AC-5 is selected, or HIGH otherwise.
42	DACK3	-	Not used
43	RSTOUT	OUT	<ul style="list-style-type: none"> ● Reset signal generated to the interface circuit board. ● When this signal becomes LOW, the printer controller is reset to an initial status and the print buffer is cleared. ● Normally this signal is HIGH, and the pulse width must be 50 μs or more at the receiving terminal.
44	ICS 6	OUT	Chip select signal of the slave CPU on the option board. * This signal is LOW when 8042 is selected, or HIGH otherwise.
45	IRD	OUT	I/O read signal. With the IRD signal LOW 8255AC-5 sends data or status to CPU via the data bus.
46	IWR	OUT	I/O write signal. With the IWR signal LOW 8255AC-5 receives data or control signal sent from CPU via the data bus.
47	+5(V)		+5(V) DC
48	+5(V)		+5(V) DC
49	+12(V)		Used when the IURS circuit board is mounted.
50	-12(V)		

Note: "Direction" refers to the direction of signal as viewed from the UXMCL circuit board

2) Table 2.2 CN2 pin assignment

(a) Use Data exchange between the main circuit board UXMCL and the driver circuit board UXDRV.

(b) Number of pins 50

Table 2.2 Pin assignment (CN2 of UXMCL)

Signal Pin No.	Signal	Direction	Description
1	H24	OUT	Print head # 24 control signal
2	H21	OUT	Print head # 21 control signal
3	H11	OUT	Print head # 11 control signal
4	H14	OUT	Print head # 14 control signal
5	H5	OUT	Print head # 5 control signal
6	H8	OUT	Print head # 8 control signal
7	H17	OUT	Print head # 17 control signal
8	H2	OUT	Print head # 2 control signal
9	H7	OUT	Print head # 7 control signal
10	H20	OUT	Print head # 20 control signal
11	H4	OUT	Print head # 4 control signal
12	H1	OUT	Print head # 1 control signal
13	H10	OUT	Print head # 10 control signal
14	H23	OUT	Print head # 23 control signal
15	H15	OUT	Print head # 15 control signal
16	H3	OUT	Print head # 3 control signal
17	H12	OUT	Print head # 12 control signal
18	H18	OUT	Print head # 18 control signal
19	H6	OUT	Print head # 6 control signal
20	H9	OUT	Print head # 9 control signal
21	H19	OUT	Print head # 19 control signal
22	H22	OUT	Print head # 22 control signal
23	H13	OUT	Print head # 13 control signal
24	H16	OUT	Print head # 16 control signal
25	CRD	OUT	CR motor control signal D phase
26	CRB	OUT	CR motor control signal B phase
27	CRC	OUT	CR motor control signal C phase
28	CRA	OUT	CR motor control signal A phase
29	SPAB	OUT	CR motor control A & B phase common line current determination of constant-current circuit
30	SPCD	OUT	CR motor control C & D phase common line current determination of constant-current circuit
31	CRHOLD	OUT	CR motor hold signal. With this signal HIGH, +5V hold voltage is applied to the CR motor
32	LFHOLD	OUT	LF motor hold signal. With this signal HIGH, +5V hold voltage is applied to the LF motor.

Signal Pin No.	Signal	Direction	Description
33	LFA	OUT	LF motor control signal A phase
34	LFB	OUT	LF motor control signal B phase
35	LFC	OUT	LF motor control signal C phase
36	LFD	OUT	LF motor control signal D phase
37	PLA	OUT	Paper hold lever control signal for the auto sheet load mechanism
38	HOT1	IN	Head temperature signal 1. At temperatures of 100°C or above, the voltage surpasses the comparison voltage of about 2.7V of the comparator.
39	HOT2	IN	Head temperature signal 2
40	+5(V)		+5V DC
41	GND		Logic ground
42	GND		Logic ground
43	PE	IN	<ul style="list-style-type: none"> ● DC Level signal to indicate the end of paper ● Normally the signal is LOW, and becomes HIGH when paper is gone.
44	MTS	IN	CR motor phase switching timing signal
45	DTS	IN	Print timing signal
46	GND		
47	SFAN	—	Not used
48	Vp		+24V DC
49	$\overline{\text{HDBRK}}$	In	This signal is LOW when current is flowing through the head pin drive coil, or HIGH otherwise.
50	Gp		+24V DC Ground

Note: "Direction" refers to the direction of signal as viewed from the UXMCL circuit board.

3) Table 2.3 CN3 pin assignment

- (a) Use To supply power from the power supply board UXPS/PSU 24E to the main circuit board UXMCL.
- (b) Number of pins 9

Table 2.3 Pin assignment (CN3 of UXMCL)

Signal Pin No.	Signal	Direction	Description
1	Vx	IN	+5V DC output when stable voltage of +24V or +5V is supplied.
2	+12V	IN	+12V DC
3	-12V	IN	-12V DC
4	+5V	IN	+5V DC
5	+5V	IN	+5V DC
6	GL	-	Logic ground
7	GL	-	Logic ground
8	PWD	IN	This signal becomes LOW when supply voltage of +24V or +5V has become unstable.
9	PSCUT	Out	Power supply cut signal. Low: Normal operating condition. High: When there is a problem with the print head or a driver transistor is defective.

Note: "Direction" refers to the direction of signal as viewed from the UXMCL circuit board.

4) Table 2.4 CN4 pin assignment

- (a) Use Signal exchange between the control panel on the UXMCL circuit board.
- (b) Number of pins 8

Table 2.4 Pin assignment (CN4 of UXMCL)

Signal Pin No.	Signal	Direction	Description
1	GL	-	Logic ground
2	SLSW	IN	Auto sheet load signal
3	LFSW	IN	Line feed signal
4	FFSW	IN	Form feed signal
5	ONSW	IN	ON/OFF line signal
6	RDY LP	OUT	READY LED drive signal
7	PELP	OUT	Paper end LED drive signal
8	ON LINE	OUT	ON LINE LED drive signal

Note: "Direction" refers to the direction of signal as viewed from the UXMCL circuit board.

5) Table 2.5 CN5 pin assignment

- (a) Use Exchange of head/home position signals between the printer mechanism Model-3660 and the main circuit board.
- (b) N u m b e r o f p i n s 4

Table 2.5 Pin assignment (CN5 of UXMCL)

Signal Pin No.	Signal	Direction	Description
1	GND	-	HOME (HP) sensor GND
2	HOME	IN	Signal from HOME (HP) sensor. This signal is HIGH when the carriage is at the home position.
3	GND	-	HOME (HP) sensor GND
4	HLED	OUT	HP sensor LED power supply

Note: "Direction" refers to the direction of signal as viewed from the UXMCL circuit board.

2.3.2 Connector on UXDRV circuit board

1) Table 2.6 CN1 pin assignment

- (a) Use To supply power from the power supply board UXPS/PSU 24E to the driver circuit board UXDRV.
- (b) N u m b e r o f p i n s 4

Table 2.6 Pin assignment (CN1 of UXDRV)

Signal Pin No.	Signal	Description
1	+24V	+24V DC head pin drive
2	+24V	+24V DC
3	Gp	+24V DC power supply GND
4	Gp	+24V DC power supply GND

2) Table 2.7 CN2 pin assignment

- (a) Use Data exchange between the driver circuit board and the Model-3660 printer mechanism.
- (b) Number of pins 34

Table 2.7 Pin assignment (CN2 of UXDRV)

Signal Pin No.	Signal	Direction	Description
1	SHIELD	-	Power supply ground
2	HD24	OUT	Print solenoid # 24 drive signal
3	TF	IN	Signal from the front head temperature sensor (HOT 1)
4	HD12	OUT	Print solenoid # 12 drive signal
5	TCOM	OUT	Temperature sensor common line +5V supply

Signal Pin No.	Signal	Direction	Description
6	HD18	OUT	Print solenoid # 18 drive signal
7	TR	IN	Signal from the rear head temperature sensor (HOT 2)
8	HD9	OUT	Print solenoid # 9 drive signal
9	HD11	OUT	Print solenoid # 11 drive signal
10	HD2	OUT	Print solenoid # 2 drive signal
11	HD21	OUT	Print solenoid # 21 drive signal
12	HD7	OUT	Print solenoid # 7 drive signal
13	HD15	OUT	Print solenoid # 15 drive signal
14	HD23	OUT	Print solenoid # 23 drive signal
15	HD6	OUT	Print solenoid # 6 drive signal
16	HDCOM	OUT	Print solenoid common line
17	HD20	OUT	Print solenoid # 20 drive signal
18	HDCOM	OUT	Print solenoid common line
19	HD5	OUT	Print solenoid # 5 drive signal
20	HDCOM	OUT	Print solenoid common line
21	HD10	OUT	Print solenoid # 10 drive signal
22	HD3	OUT	Print solenoid # 3 drive signal
23	HD17	OUT	Print solenoid # 17 drive signal
24	DH	OUT	Print solenoid # 1 drive signal
25	HD	OUT	Print solenoid # 19 drive signal
26	HD13	OUT	Print solenoid # 13 drive signal
27	HDCOM	OUT	Print solenoid common line
28	HD16	OUT	Print solenoid # 16 drive signal
29	HDCOM	OUT	Print solenoid common line
30	HD22	OUT	Print solenoid # 22 drive signal
31	HDCOM	OUT	Print solenoid common line
32	HD8	OUT	Print solenoid # 8 drive signal
33	HD14	OUT	Print solenoid # 14 drive signal
34	HD4	OUT	Print solenoid # 4 drive signal

Note: "Direction" refers to the direction of signal as viewed from the UXDRV circuit board.

3) CN3 pin assignment

Refer to Table 2.2.

4) Table 2.8 CN4 pin assignment

- (a) U s e Exchange of carriage motor signals between the drive circuit board and the Model-3660 printer mechanism.
 (b) Number of pins 18

Table 2.8 Pin assignment (CN4 of UXDRV)

Signal Pin No.	Signal	Direction	Description
1	OCRA	OUT	CR motor drive signal A phase
2	OCRB	OUT	CR motor drive signal B phase
3	CMAB	OUT	CR motor drive A & B common line
4	OCRC	OUT	CR motor drive signal C phase
5	OCRD	OUT	CR motor drive signal D phase
6	CMCD	OUT	CR motor drive C & D common line
7	NC	-	Not used
8	+5V	OUT	DTS sensor power (+5V)
9	DLED	OUT	DTS sensor LED power
10	IDTS	IN	DTS sensor signal
11	GND	-	DTS sensor ground
12	GND	-	DTS sensor shield
13	NC	-	Not used
14	+5V	OUT	MTS sensor power (+5V)
15	MLED	OUT	MTS sensor LED power
16	IMTS	IN	MTS sensor signal
17	GND	-	MTS sensor ground
18	GND	-	MTS sensor shield

Note: "Direction" refers to the direction of signal as viewed from the UXDRV circuit board

5) Table 2.9 CN5 pin assignment

- (a) Use..... Exchange of control signals between the drive circuit board and the Model-3660 printer mechanism for paper feed motor or paper hold release plunger.
- (b) Number of pins 12

Table 2.9 Pin assignment (CN5 of UXDRV)

Signal Pin No.	Signal	Direction	Description
1	OLFA	OUT	Paper feed motor A phase
2	OLFB	OUT	Paper feed motor B phase
3	OLFC	OUT	Paper feed motor C phase
4	OLFD	OUT	Paper feed motor D phase
5	LFCOM	OUT	Paper feed motor common line (+24V)
6	LFCOM	OUT	Paper feed motor common line (+24V)
7	+24V	OUT	Paper hold release plunger (+) (+24V)
8	PLNGR	OUT	Paper hold release plunger (-) (+24V)
9	NC	-	Not used
10	+5V	OUT	Paper end sensor power (+5V)
11	$\overline{\text{IPE}}$	IN	Paper end sensor signal
12	GND	-	Paper end sensor ground

Note: "Direction" refers to the direction of signal as viewed from the UXDRV circuit board.

6) Table 2.10 CN6 pin assignment

- (a) Use To supply power to the fan set UA from the driver circuit board.
- (b) Number of pins .. 2

Table 2.10 Pin assignment (CN6 of UXDRV)

Signal Pin No.	Signal	Description
1	FAN 1 +	Fan power +24V
2	FAN 1 -	Fan power ground

7) Table 2.11 CN7 pin assignment

- (a) Use Connection of the driver circuit board and the ceramic resistance
- (b) N u m b e r o f p i n s 2

Table 2.11 Pin assignment (CN7 of UXDRV)

Signal Pin No.	Signal	Description
1	+24V	Cement resistance connection terminal
2	HLDR	Cement resistance connection terminal

2.3.3 Connector on UXPS/PSU 24E circuit board

1) CN1 pin assignment

AC power is supplied from UXFIL circuit board

2) CN2 pin assignment

Refer to 2.3.1 3) Table 2.3

3) CN3 pin assignment

Refer to 2.3.2 1) Table 2.6

4) Table 2.12 CN4 pin assignment

(a) Use To supply power from the UXPS/PSU 24E circuit board to the fan set UB.

(b) Number of pins 2

Table 2.12 Pin assignment (CN4 of UXPS/PSU 24E)

Signal Pin No.	Signal	Description
1	FAN +	Fan power +24V
2	FAN -	Fan power ground

2.4 Electrical Circuits

2.4.1 Power circuit

Overview

The power supply circuit of the LQ-1500 consists of a fuse and filter circuit and power supply circuit.

The output voltages are +5, +12 and -12V for logic circuits and +24V for printer drive.

The power supply circuit, employs a switching power supply system in which the input voltage is directly rectified for use.

Table 2.13 Voltage utilization

Output	Voltage Range	Nominal Current	Use
+5 Include Vx	4.9 ~ 5.1V	2.5A	Logic circuit
+24	23.3 ~ 25.7V	6.0A	Printer drive
+12	11.7 ~ 13.3V	0.15A	RS-232C, Power for DRAM
-12	11.7 ~ 13.3V	0.15A	RS-232C, Power for DRAM

[A] 100V/120V version circuit

1. Noise filter circuit (100/120V version)

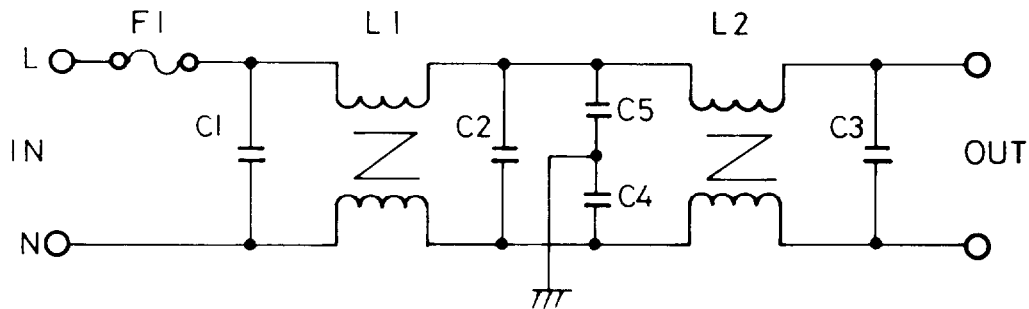


Fig. 2.3 Noise filter circuit

The noise filter circuit is mounted on the UXFIL board together with the fuse. Incoming AC flows through the power switch and fuse before being filtered by a noise suppression circuit on the UXFIL board. The filter circuitry limits electrical interference both to and from the printer.

2. Rectifying circuit and inrush current prevention circuit (100/120V version)

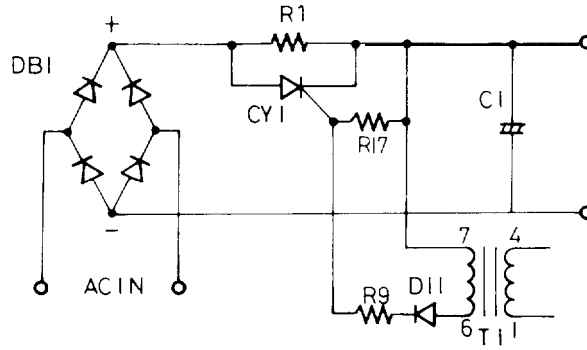


Fig. 2.4 Rectifying circuit and inrush current prevention circuit

In this power supply system, the AC input is directly rectified by the diode bridge DB1 and the output voltages are as shown above.

An explosion-proof valve is provided in the upper part of the case of smoothing condenser C1. If an abnormal voltage is applied to C1, the explosion-proof valve will open, rendering the part inoperative.

In this power supply system, an inrush current flows at power on. Immediately after power on, when C1 is not charged, an excessive charging current that may flow can cause the trouble of fuse F1 or DB1. To prevent it, R1 limits the inrush current. In other words, C1 is charged through R1 at the time of power on. With the start of power supply, a voltage is generated at the output of transformer T1, and this is rectified by D11 and thyristor CY1 is triggered. Now the thyristor shorts both the ends of R1, thus completing the action of preventing Inrush current. The thyristor is conducting electricity as long as the power supply is on.

When the thyristor does not conduct electricity because of some trouble, the power supply remains normal, but R1 gets heated abnormally. Also, R1 may sometimes be disconnected when fuse F1 is blown.

3. Converter circuit (100/120V version)

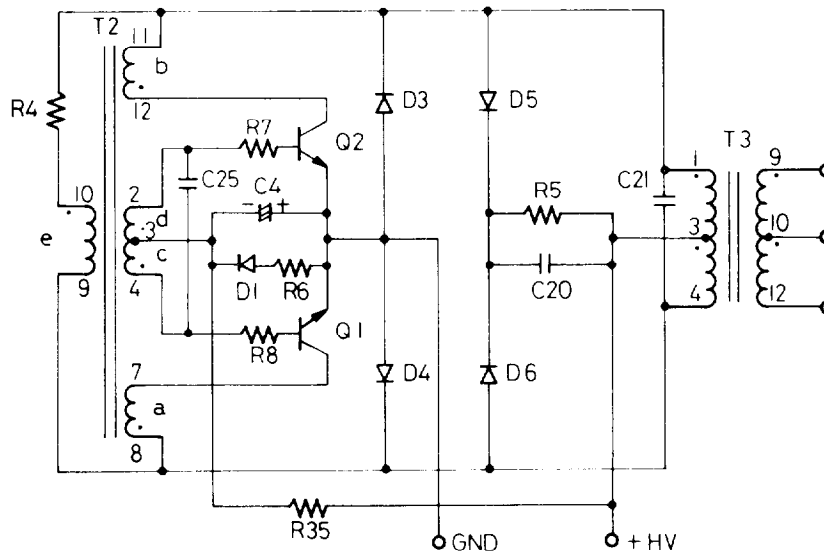


Fig. 2.5 Converter circuit

In this circuit, transistors Q1 and Q2 alternately supply current to the windings of transformer T3, producing AC voltage as the output. 50/60 Hz input is frequency converted into 20 kHz through the action of pulse transformer T3. This circuit starts oscillating automatically at about 20 kHz by transformer T2. With the power supply on, R35 causes the base current to flow and either Q1 or Q2 turns on. Once started, the base current is supplied from windings a and b, so that the transistor, which has been off, turns on instantly. T2, which is a current transformer, is in a positive feedback connection. 1/10 of the collector current from windings c and d as the base current. Oscillation frequency is determined by the length of time it takes the core of T2 to become magnetically saturated after excitation from windings a and b.

When this occurs, the transistor which has been of opposite polarity is generated at T3.

Winding e adds this voltage to the base current and thus prepares the transistor which has been off, to turn on. Then oscillation continues, with the trigger voltage from winding e applied to Q1 and Q2 alternately. R4 limits the current that flows to winding e.

The voltage drop caused by R6 and D1 is smoothed by C4 to produce an inverse bias voltage when Q1 or Q2 turns off. D3 and D4 are used as the by-pass when part of the magnetic energy is returned to the input power. D5 and D6 clamp the spike voltage generated by T3 at switching to the DC input voltage via R5 and C20.

The clamp voltage is about twice as large as the DC input voltage. C21 reduces the transitional switching loss of Q1 and Q2. Q1 and Q2 are parts most liable to develop failure.

Note: When troubleshooting the power supply, Q1 and Q2 should be among the first check points. When either of these transistors are isolated as a trouble source, both must be replaced. Replacing only one of the transistors can result in continued problems.

4. Power transformer circuit (100/120V version)

The variable leakage transformer not only performs power transformation by insulating the load from higher voltage, but also stabilizes the output voltage by controlling the current flow to the control winding. The VLT raises the DC output voltage by sending DC current into control winding f. From this current, the VLT outputs a stabilized waveform.

With 20 kHz AC voltage applied to the input windings a and b, the pulse-width controlled AC voltage can be obtained from the windings c and d. The winding e, which is an auxiliary power source of about 9V, is used to drive the control winding f.

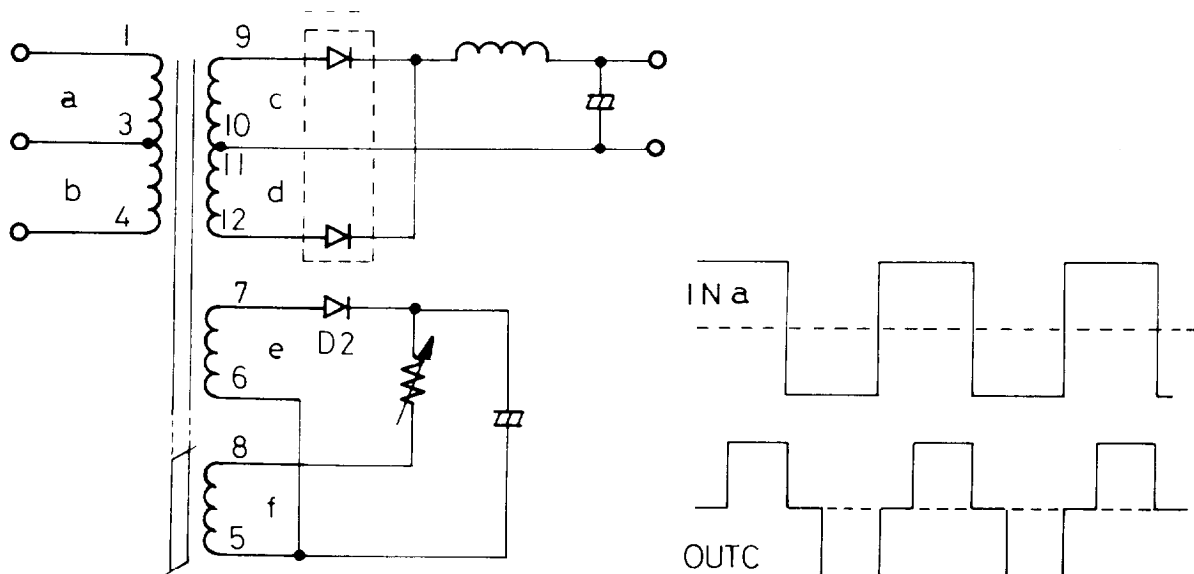


Fig. 2.6 Power transformer circuit

5. +24V output circuit (100/120V version)

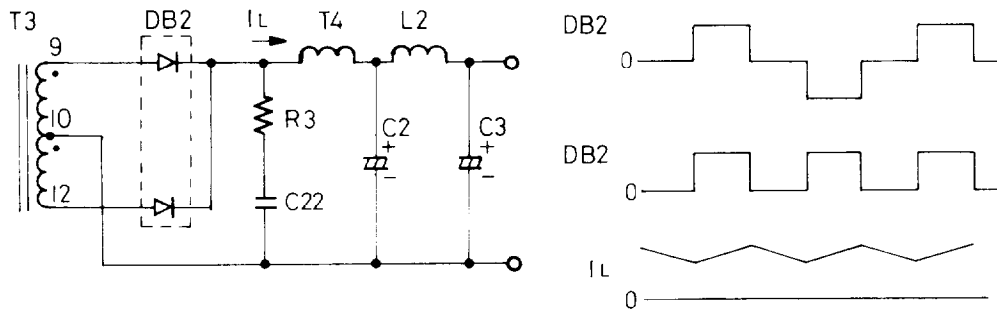


Fig. 2.7 +24V output circuit

The +24V output circuit is capable of supplying an average current of 6A. In this circuit, the pulse-width controlled voltage from VLT is rectified and smoothed. The output which is a pulse voltage, rectified by DB2 is smoothed by choke coil T4 and C2, so a continuous load current flows.

T4, excited by the output voltage of DB2, stores magnetic energy. When the current stops flowing from the VLT, T4 discharges the magnetic energy, so the load current flows continuously.

C22 and R3 prevent the spike voltage from occurring as a result of rectification. L2 and C3 constitute a spike prevention filter.

6. Output control circuit (100/120V version)

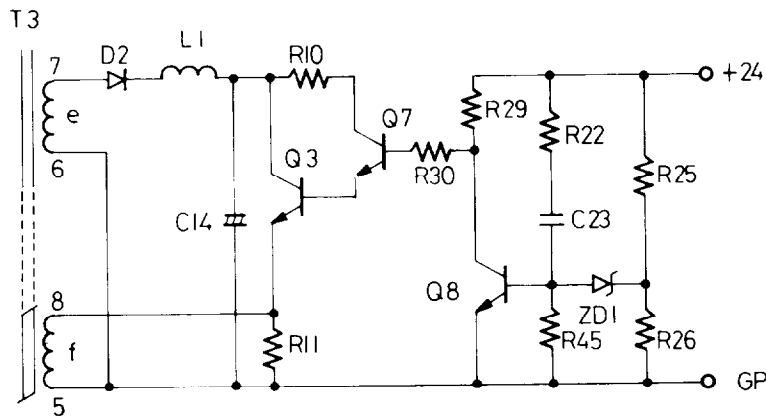


Fig. 2.8 Output control circuit

In this circuit, the output voltage is detected and the output is stabilized by controlling the current flowing to the control winding f of VLT. The current to the control winding is supplied from e, which is the auxiliary power source, and is driven by Q3 and Q7.

The output voltage is detected by zener diode ZD1. A constant output voltage is maintained which adjusts the base current of Q7 as assuring a constant current flow to ZD1.

If too much current flows to winding f as a result of machine malfunction, the system is short circuited, winding f is cut off and output drops below 12V.

R22 and C23 advance the phase so as to maintain a stable output voltage. L1 and C14 constitute an auxiliary power source smoothing filter.

7. Output cutoff circuit (100/120V version)

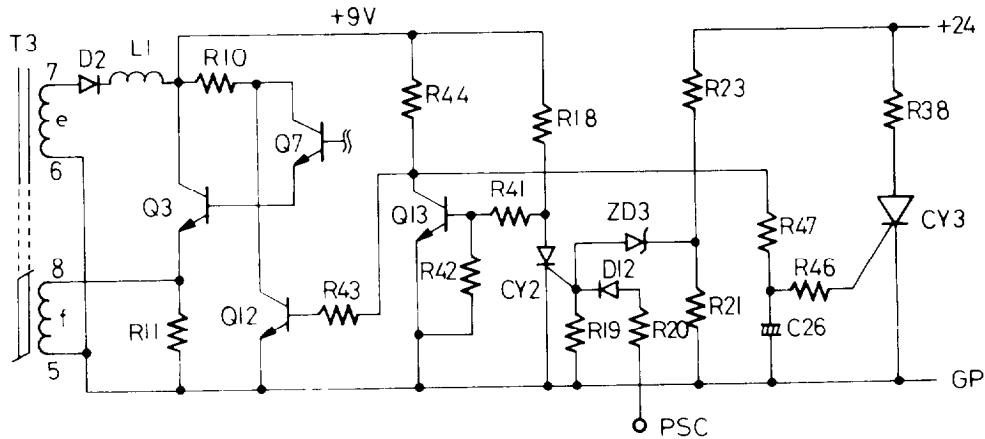


Fig. 2.9 Output cutoff circuit

The output cutoff circuit is activated when the PSC signal is input or 30V or more is output as a result of a malfunction.

When the thyristor CY2 is kept on, Q13 turns on Q12 and stops the base current of Q3, so that power is not supplied to the control winding of VLT. Then +24V output is shorted by triggering the thyristor CY3. A PSC signal is output due to failure of a printhead drive transistor.

8. DC-DC converter (100/120V version)

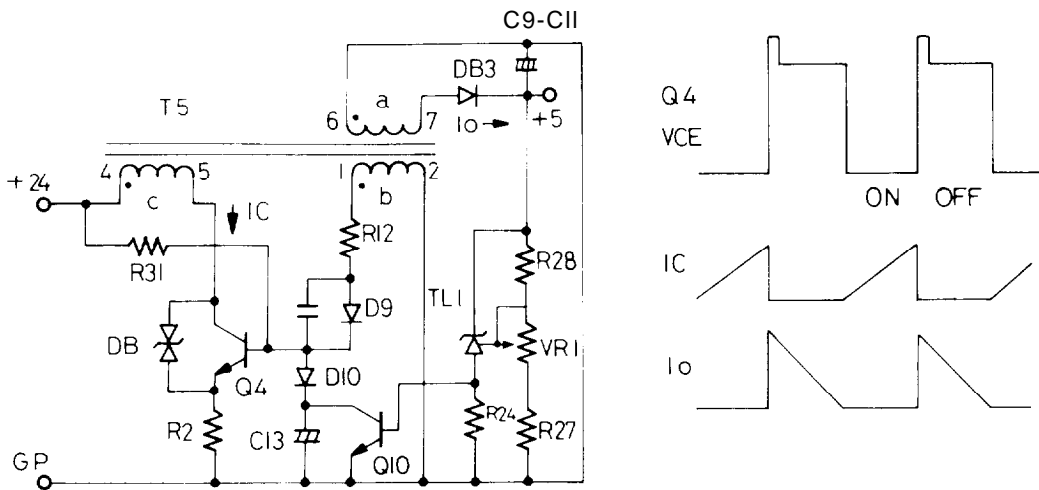


Fig. 2.10 DC-DC converter circuit

In this circuit, outputs of +5, +12 and -12V are produced from +24V.

This circuit starts oscillating automatically at power on.

As the base current flows through R31 and Q4 turns on. With winding c excited, an electromotive force is generated in winding b. Q4 turns on quickly because positive feedback of the voltage in winding b is made to the base current of Q4.

With Q4 switched on, the current flowing to winding c continues increasing until it is restricted by the base current value.

Q4 is turned off quickly by a counterelectromotive force generated in winding b, when increase in collector current stops.

The magnetic energy stored in transformer T5 during the ON period is discharged to the load side during the OFF period. When the magnetic energy is discharged, the counterelectromotive force in winding b is lost and Q4 starts turning on again. The output is stabilized by controlling the average current flowing to the winding c.

As +5V output begins to rise, the current flowing into the winding c is reduced, and as it begins to drop, the current flowing into the winding c is increased. These controls are performed with Q10 shunting the base current flowing to Q4. The voltage detector TL1 adjusts the base current of Q10 to maintain the +5V output constant.

The oscillation frequency of the circuit lowers with more load current or rises with less load current.

Under no load, the oscillation becomes intermittent. Normally the circuit operates at about 30 kHz.

D10 and C13 rectify and smooth the base voltage of Q4.

D13, which is a two-way zener diode, clamps the surge voltage generated by T5 to 68V to protect Q4.

VR1 is used to set the +5V output voltage.

9. +5V output circuit (100/120V version)

+5V output is used for the logic circuit.

The current flowing through DB3 charges C9 through 11. The extremely large current value, however causes a large output voltage ripple which is smoothed by Ls and C12.

10. 12V output circuit (100/120V version)

12V output, which is not stable, is used by RS-232C.

Since the DC-DC converter stabilizes the output by detecting +5V, the output voltage drops to about 5V when +5V is under no load.

11. Vx. PWD circuit (100/120V version)

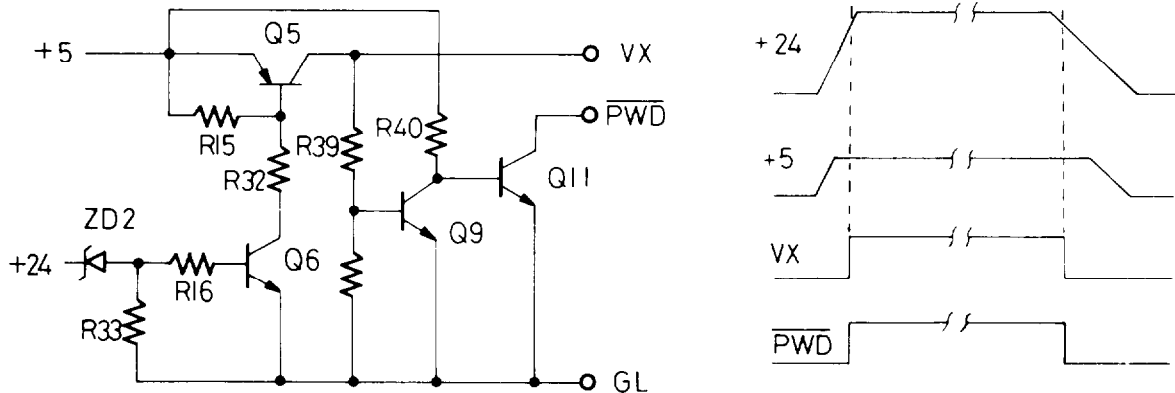


Fig. 2.11 Vx. PWD

Vx is output when +5V and +24V voltages become stabilized and is used to prevent the misoperation of the printer when the power supply is turned on or off.

+5V make from +24V, retains the stable condition longer than +24V. Therefore, Vx is output when the +24V output is +21 V or above.

A voltage drop on the +24V line due to a power failure or machine malfunction turns Q11 on and triggers the PWD signal. When PWD is output the CPU is reset and the printer is stopped.

[B] 220/240V version circuit

1. Noise filter circuit (220/240V version)

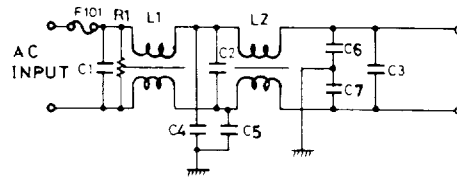


Fig. 2.12 Noise filter circuit

A switching regulator generates noise because of its circuit configuration. Each country has its own noise regulations, the circuit configuration, Fig. 2.12, is adopted to meet VDE 0871 class B.

2. Rectifying circuit, inrush current prevention circuit and converter circuit (220/240V version)

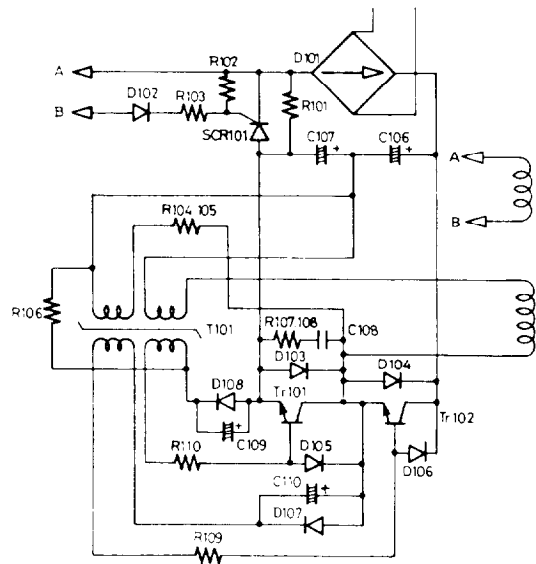


Fig. 2.13 Rectifying and converter circuit

The supply voltage passed through the noise filter circuit is rectified at D101 and smoothed at C106 and C107, providing the mid-point voltage as shown in Fig. 2.13.

R101 and SCR101 form an inrush current prevention circuit. When power is applied, the current is charged to C106 and C107 via R101 with SCR101 OFF. When the charged voltage rises, the converter oscillates, SCR101 turns ON and the current path changes from R101 to SCR101. Switching transistors Tr101 and Tr102 form a symmetric excitation half-bridge type converter which is activated by T101. The oscillation frequency depends on the saturation of T101. This converter supplies a symmetric pulse voltage to the transformer.

3. Power transformer circuit (220/240V version)

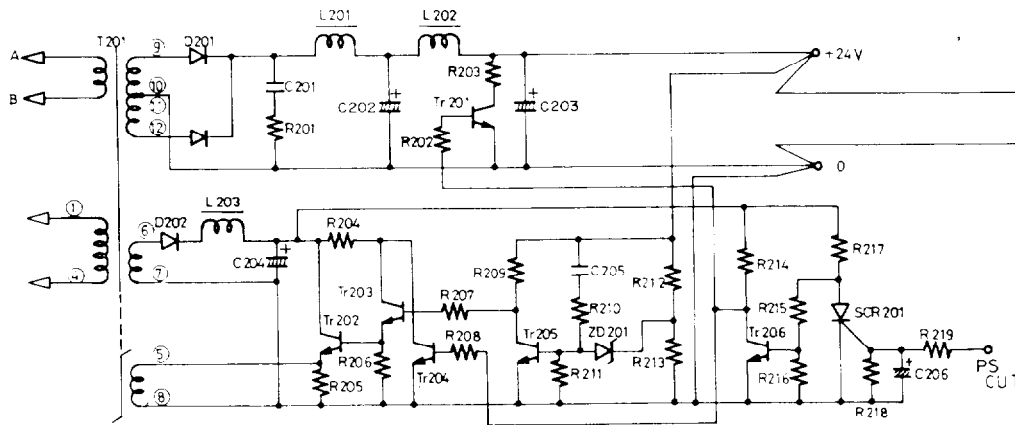


Fig. 2.14 Power transformer circuit

The transformer T102, a variable leakage transformer, has a construction capable of output control. The pulse voltage input to the primary winding (terminals 1 and 4) is controlled by the DC current flowing at the control winding (terminals 5 and 8) and is output to the secondary winding (terminals 9 - 12). As shown in Fig. 2.16, the width of the pulse output to the secondary winding increases as the control current is made larger.

Output voltage V_0 is:

$$V_0 = V_2 \times \frac{T_{ON}}{T}$$

$$V_2 = \sqrt{2E} \times \frac{N_2}{N_1}$$

thus,

$$V_0 = \sqrt{2E} \times \frac{N_2 \cdot T_{ON}}{N_1 \cdot T}$$

where, N_1 = number of turns of primary winding

N_2 = number of turns of secondary winding

T = period

T_{ON} = time during which pulse is output to secondary winding

4. +5V, ± 12 V output circuit (220/240V version)

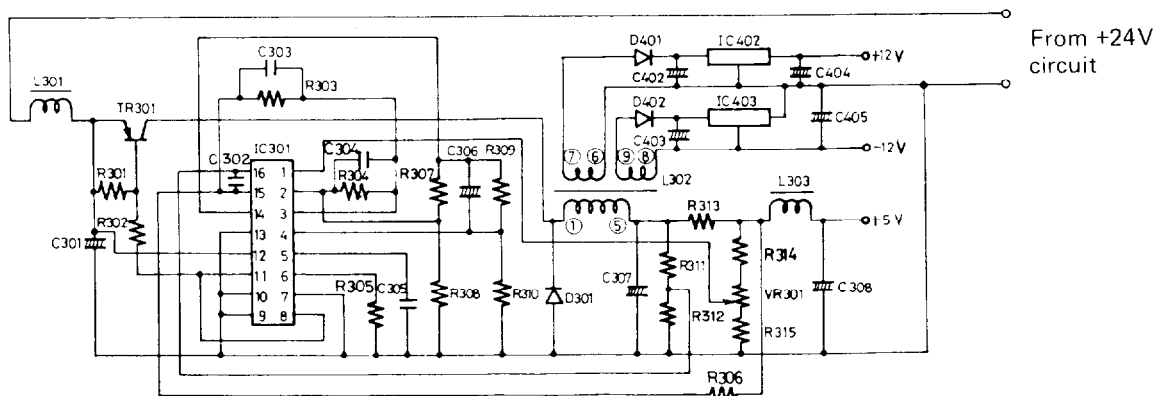


Fig. 2.15 +5V, ± 12V output circuit

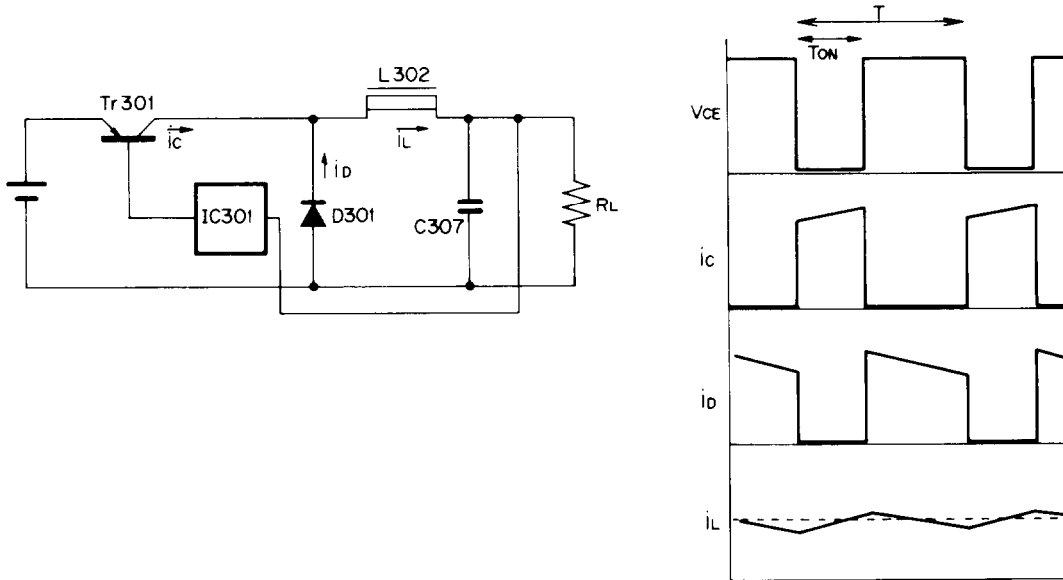


Fig.2.16 Switching regulator circuit

This circuit is formed by a chopper circuit with a power supply of +24V.

As shown in Fig.2.16. when transistor Tr301 turns ON, collector current i_c flows, supplying current to the load.

At the same time, magnetic energy is being stored in choke coil L (See T_{on} , Fig. 2.16). If transistor Tr301 turns off, collector current is also cut off. When this occurs, choke coil L maintains current flow by emitting the stored magnetic energy in the form of current, supplying the load and flywheel diode D.

Output voltage, V_{out} , is maintained at a constant level by a control IC, which constantly monitors output, and switches transistor Tr301 on or off, as required to maintain a constant output.

The relationship between the input and output voltage is expressed as:

$$V_{out} = \frac{T_{ON}}{T} \times V_{in}$$

5. V_x , PWD (Power down) circuit (220/240V version)

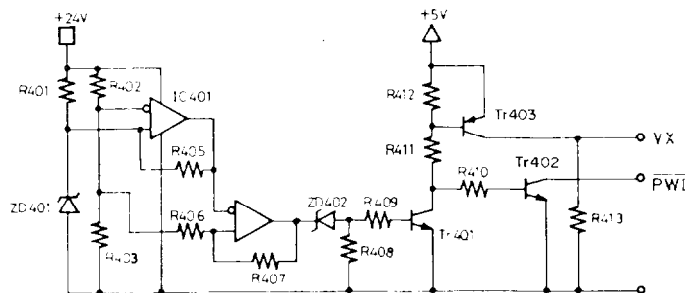


Fig.2.17 V_x , PWD circuit

This circuit compares the +24V output with the reference voltage to generate V_x .

The +24V output is divided by R402 and R403. Then, the divided voltage is compared with the reference voltage obtained by ZD401. When it exceeds 20V, TR402 turns ON and sends 5V to pin V_x . At the same time, open collector transistor TR403 turns ON.

This circuit has a slight hysteresis to prevent chattering due to ON/OFF operation.

2.4.2 Reset circuit(Fig. 2.18)

The reset signal is used to reset and start the CPU, causing It to initiate the routine which initializes the processor and associated circuitry.

The reset signal is output only in the following cases:

- 1) At power on: The signal is output for about 30 ms at the turning on of power.
- 2) By interface signal: The signal is given while the INIT signal is output from the host computer.

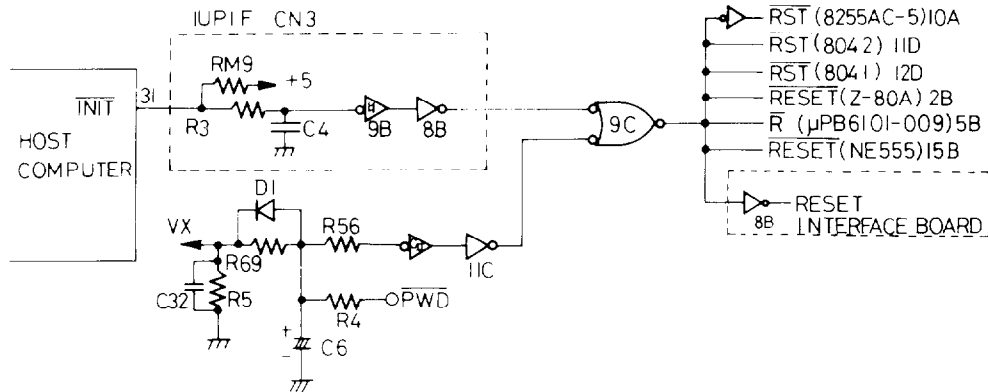


Fig. 2.18 Reset circuit

The reset signal is output at power on when Vx (+5V) is applied to the power on reset circuit, consisting of RM9, R3 and C4; it is passed on to IC 9B, pin 1, 8B and 8A, which is the reset signal port initiator.

Time constant of the reset pulse is applied at R69 and C4.

This time constant is approximately 30 ms.

Upon the input of an INIT signal from the interface board, the interface reset (INIT) signal is input to: the main CPU Z-80A; slave CPUs 8042 and 8041, PPI 8255AC-5; gate array uPB6101-009; and timer NE555. The INIT signal is output only during the system reset or I/O reset of the host computer that controls the LQ-1500.

If power is off the reset cannot be output.

2.4.3 Sensor circuit

Five sensor circuits (HP, MTS, DTS, PE and HOT1 and 2) monitor status of the printer mechanism and inform the Z80-A CPU as to the mechanism's operational status at any given time.

- 1) Home position sensor circuit (Fig.2.1 9)

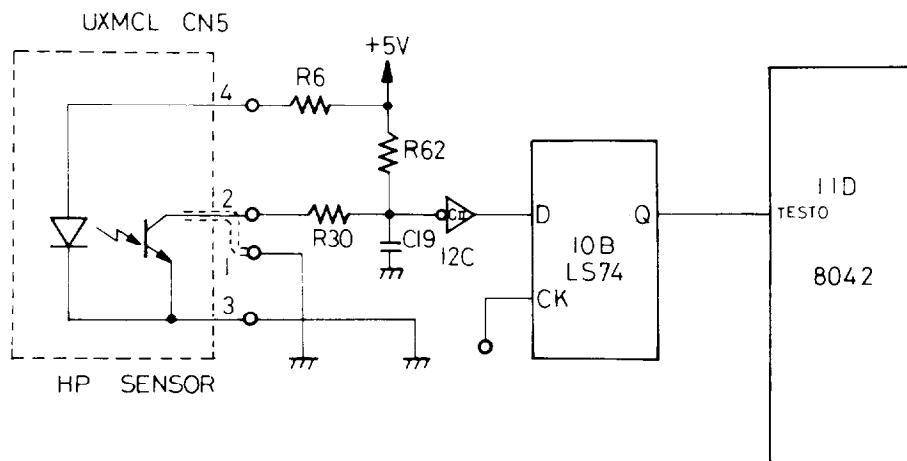


Fig. 2.19 HP sensor circuit

The home position sensor circuit detects signals defining when the printhead is in or out of the home position. The signal is read when the power switch is turned on or signal INIT is applied to the printer. This circuit also operates at the instruction of carriage return.

When the carriage is out of the home position, phototransistor turns on causing a HIGH output signal to be emitted to the CPU. At the return of the carriage to the home position, the photocoupler is screened, the phototransistor is turned off, and the output of HP drops to LOW. The carriage is in the home position, and it is notified to the 8042. The output signal from the phototransistor is integrated and input to the Schmitt circuit, which prevents the waveform of the output signal from being disturbed by noise or mechanical vibration.

2) MTS sensor circuit

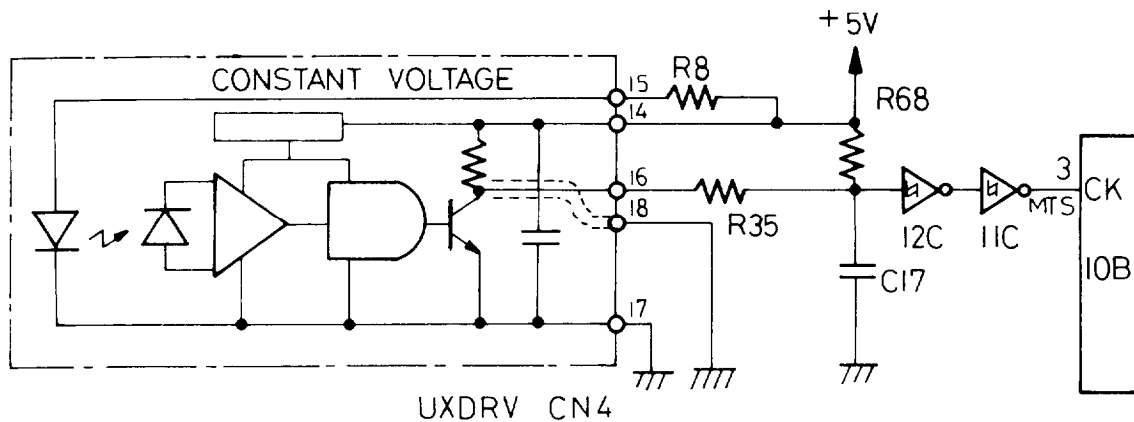


Fig. 2.20 MTS sensor circuit

The MTS sensor circuit detects the signal that defines the speed of the head carriage. When the light is screened by the slit plate (Fig. 2.21) at the photocoupler, the photodiode turns off and HIGH level voltage is applied to the transistor base of the sensor so that the transistor turns on. As a result, the MTS signal becomes LOW. When the light passes through the slit, the photodiode turns on and the transistor of the sensor turns off, so that the MTS signal becomes HIGH.

The period of MTS signal is 860s in the draft mode and 2.52 ms in the letter quality (LQ) mode.

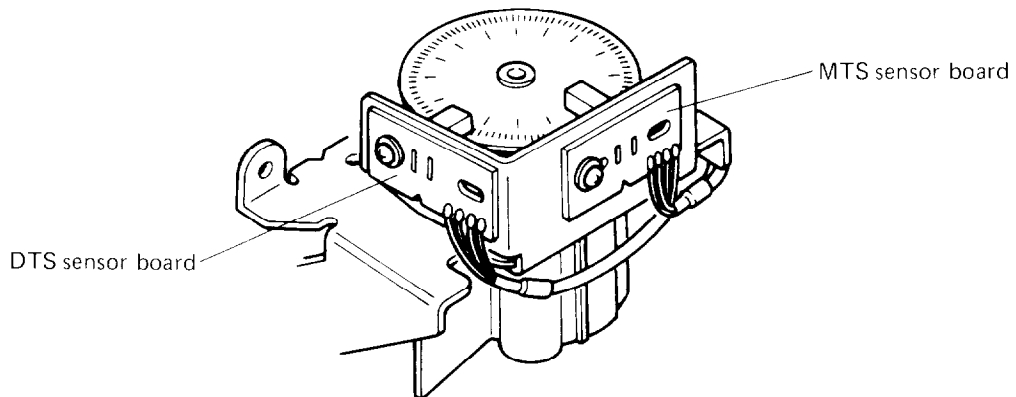


Fig. 2.21 Sensor assembly

3) DTS sensor circuit (Fig.2.22)

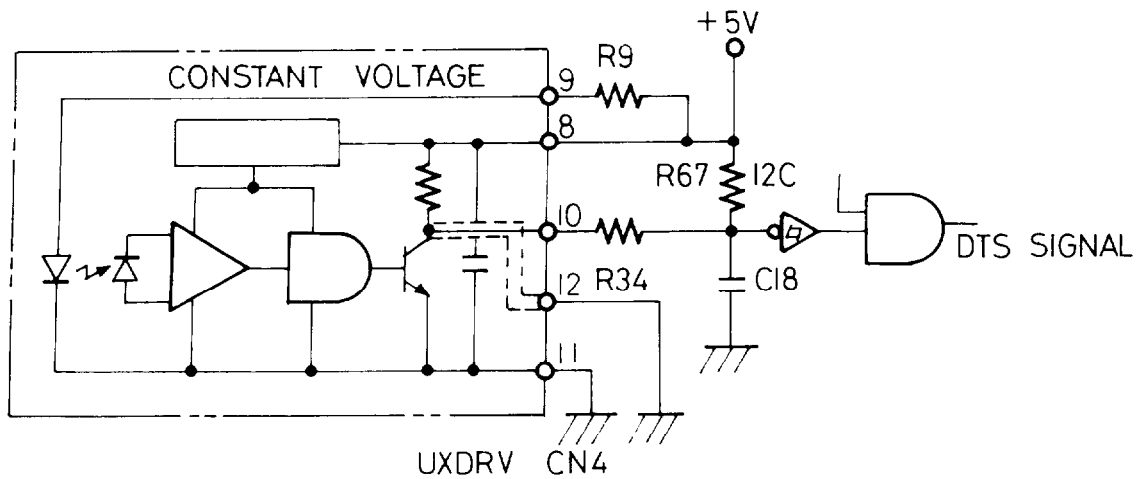


Fig. 2.22 DTS sensor circuit

The DTS sensor circuit detects the print timing signal. This signal comes in three pulses in one period of MTS. As shown in Fig. 2.22, it operates the same way as the MTS sensor circuit.

The timing of DTS signal is 287s in the draft mode and 840s in the letter quality (LQ) mode.

4) Paper end sensor circuit (Fig.2.23)

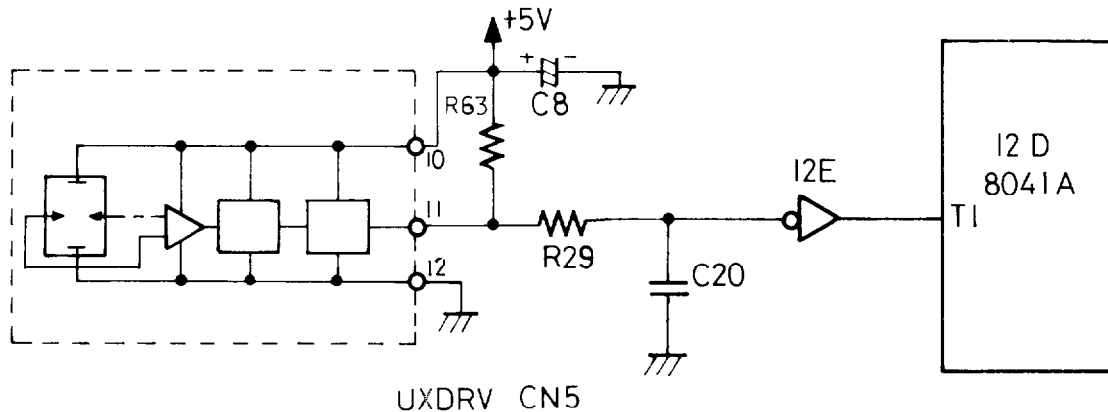


Fig. 2.23 PE sensor circuit

The paper end sensor circuit employs a magnet-electricity conversion system using a Hall IC; output is of the open collector type. The output signal from the sensor is integrated once and input to the Schmitt circuit, which prevents the waveform of the output signal from being disturbed by noise or mechanical vibration.

When paper has been inserted in the mechanism, the Hall IC is off and pulled up by R63, so that the output of PE signal is LOW. When the paper is gone, the Hall IC goes on and the collector drops to ground level, so that the output of PE signal becomes HIGH. The PE signal is applied to T1 (pin 39) of CPU8041 A. It is possible to render the PE signal ineffective via a control code or DIP switch setting.

The RE sensor will be ignored and the error signal will not function when DIP switch 2-2 is set or an ESC 8 control code is input. In this mode of operation, although the PE LED goes on, the READY LED remains on and data can still be received.

* See the operating manual for an explanation of DIP switch settings and use of control codes.

5) Head temperature sensor circuit (Fig. 2.24)

Overheating of the print head during heavy duty printing operation is prevented by the head temperature sensor circuit.

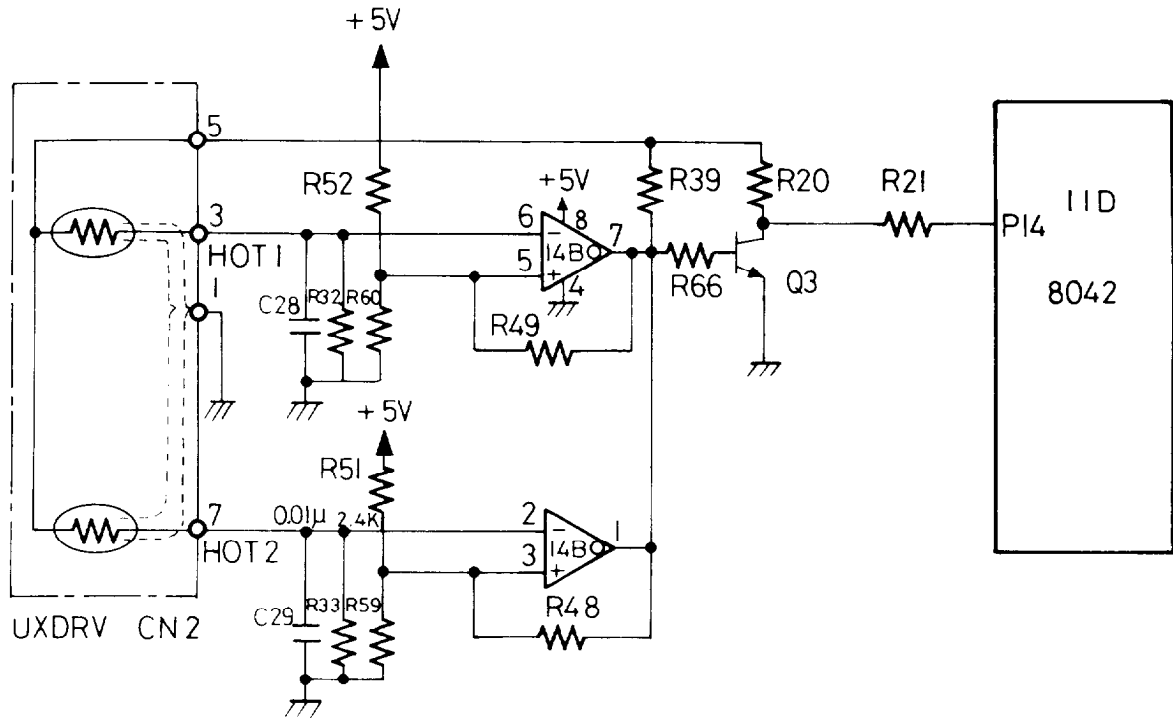


Fig. 2.24 Head temperature sensor circuit

The head temperature sensor circuit detects the temperature of the print head unit

A fan, situated at home position circulates air, providing a cooling system.

As the temperature of the print head unit reaches approximately 100°C or above, the printing is halted temporarily and the print head unit is returned to the home position.

A thermistor provided in the print head unit is pulled up to 5V. As the temperature of the unit rises, the resistance decreases and the voltage at the negative terminal (HOT1, HOT2) of the comparator rises higher than the positive terminal of the comparison voltage.

As the output terminal becomes LOW, Q3 switches from on to off, and the collector level moves from LOW to HIGH.

2.4.4 Carriage motor control circuit (Figs. 2.25.26)

The control signal of the carriage motor is output from 8042 of the main circuit board. The signal is first received by the transistor array and then driven by the regulator IC STK6982 (IC2).

The 2-2 phase carriage motor runs in combinations of phases A to D. (See Table 2.14 and Fig. 2.25.)

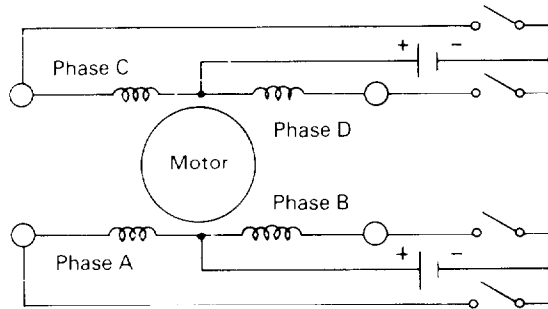


Fig. 2.25 Motor circuit

The belt, motor sequence for driving the timing belt is shown below.

Table 2.14 Carriage motor step sequence

Carriage	Step	Phase A	Phase B	Phase C	Phase D
From left to right	1	ON	OFF	ON	OFF
	2	ON	OFF	OFF	ON
	3	OFF	ON	OFF	ON
	4	OFF	ON	ON	OFF
From right to left	1	ON	OFF	OFF	ON
	2	ON	OFF	ON	OFF
	3	OFF	ON	ON	OFF
	4	OFF	ON	OFF	ON

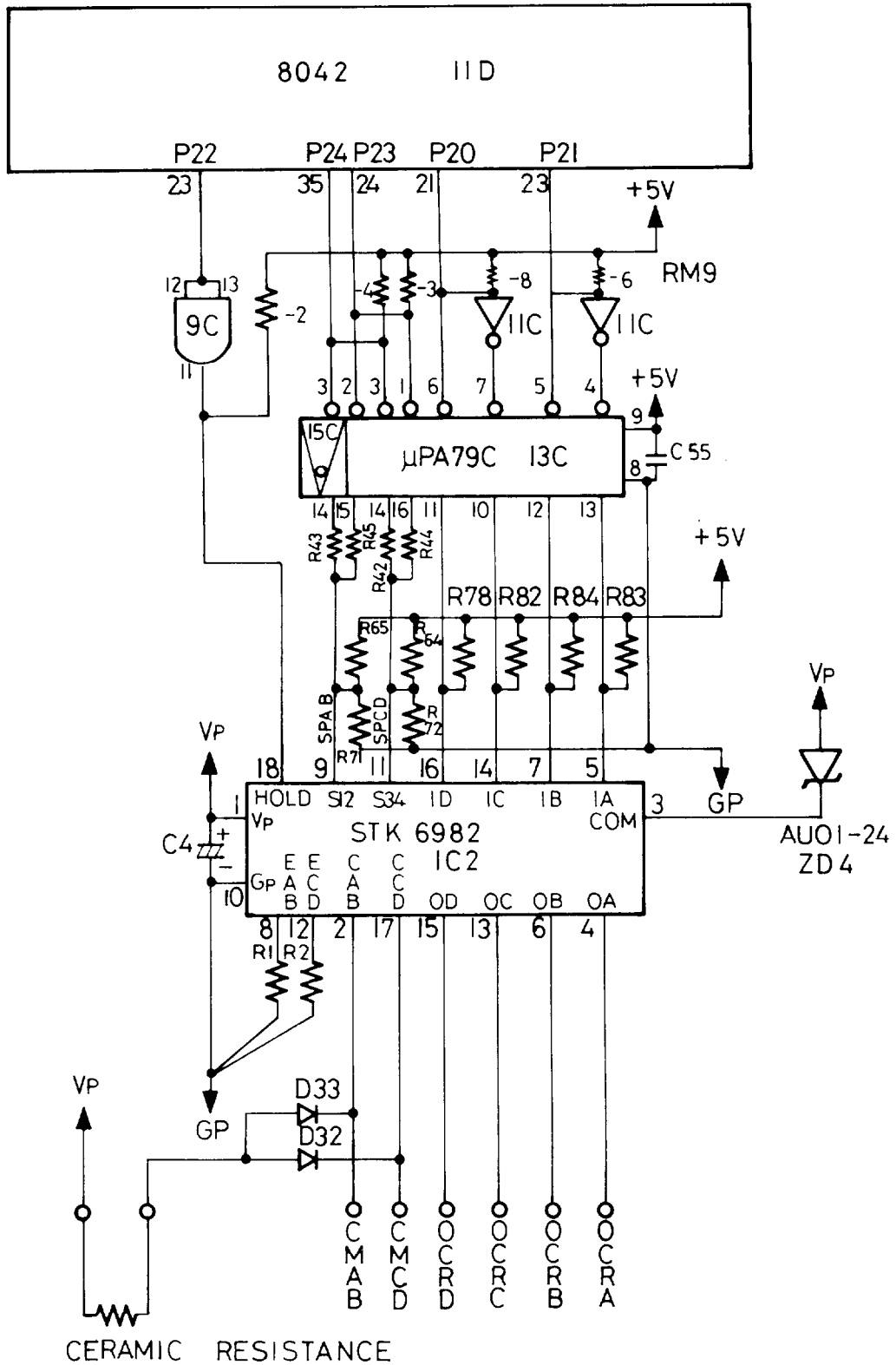


Fig. 2.26 CR motor drive circuit

The phase changing signal for the carriage motor is output from P20 and P21 of CPU 8042. The control signal of phases A and B is inverted via the phase inverter, 1 1 C, and used as the control signal of phase C and phase D, respectively.

Power supply to the carriage motor is monitored by resistances R1 and R2 connected to the EAB and ECD terminals of STK6982, and the outputs of CAB and CCD are controlled in accordance with the reference voltages S12 and S34 of the comparator inside STK6982. Accordingly, the speed of the carriage motor can be changed by changing this reference voltage; reference voltage changes depending on whether the resistances R42 and R43 or R44 and R45, connected to the transistor array by the output of P23 and P24 of 8042, are selected. Also, ZD4 is provided to prevent counterelectromotive force. Power supply to the motor is such that switching to high speed can be made by STK6982. The electric energy stored in each coil is discharged following the end of power supply there, which can cause the breakdown or malfunction of the elements. To prevent it, the energy produced by the counterelectromotive force is released through the zener diode.

When the output of P22 of 8042 is HIGH, the HOLD terminal of STK6982 is HIGH. Therefore the common line is cut off from 24V power supply and, instead, the power is supplied from Vp via the cement resistances D32 and D33. And the current flows through all the phases simultaneously, thus putting the carriage motor in a HOLD state.

Control method:

The Model-3660 carriage drive motor can be stopped at any position by controlling acceleration/ deceleration and the alternation of print direction.

A closed loop control method is used in which the MTS timing signal is fed back to the pulse motor drive phase switching.

Closed loop control:

The motor phase switching is made by comparing the MTS output from the printer to the control time setting.

When the MTS period, compared with the time setting, is longer, the CR motor phase switching is made at the leading edge of MTS. (See Fig. 2.27.)

When the MTS time setting is shorter, MTS is output within the time setting, though the CR motor phase switching is not made at this time, but after the lapse of the time setting. (See Fig. 2.27.)

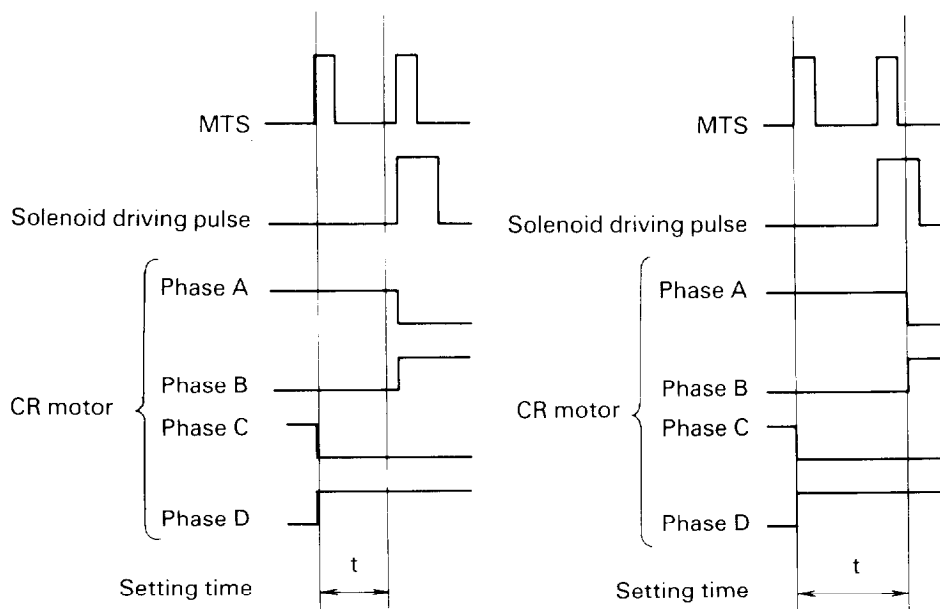


Fig. 2.27 MTS timing

(1) Motor bias voltage

The bias voltage for the motor is of two kinds; one for operation use and the other for non-operation use.

Table 2.15 Motor bias voltage

Mode	Voltage	Use
Operation	+24V ± 10%	Driving of motor
Non-operation	+5	Holding bias

(2) Carriage motor drive signal timing

(a) Acceleration control and constant speed control

For acceleration control and constant speed control, the following time settings (Table 2.16) are available in the printing speed (CR motor speed) modes of 1163 pps, 769 pps, 592 pps and 397 pps:

Table 2.16 Speed control table

Mode *1	1163 pps	769 pps	592 pps	397 pps
tC1	5.00	5.00	6.72	7.48
tC2	2.72	3.16	4.08	5.48
tC3	2.16	2.64	3.40	4.40
tC4	1.80	2.32	2.96	3.76
tC5	1.56	2.08	2.60	3.36
tC6	1.40	1.88	2.36	3.12
tC7	1.32	1.76	2.20	2.92
tC8	1.24	1.68	2.04	2.84
tC9	1.16	1.60	1.96	2.76
tC10	1.08	1.52	1.92	2.68
tC11	1.00	1.48	1.88	2.64
tC12	0.92	1.44	1.84	2.60
tC13	0.88	1.40	1.80	2.56
tC14	0.88	1.36	1.76	2.56
tC15	0.88	1.32	1.72	2.56
tC16	0.88	1.32	1.72	2.56
tC17	0.88	1.32	1.72	2.56
tC18	0.88	1.32	1.72	2.56
Constant Speed	0.88	1.32	1.72	2.56

(b) Deceleration control (Table 2.17)

The MTS period (TDo) immediately before the start of deceleration control is measured, and the following deceleration controls are made depending on the TDo value and the CR motor speed mode:

1. Deceleration mode A: Used when the CR motor speed is in the 1163 pps and 769 pps modes and TDo is shorter than 1.72 ms.
2. Deceleration mode B: Used when the CR motor speed is in the 1163 pps and 769 pps modes and TDo is longer than 1.72 ms.
3. Deceleration mode B: Used when the CR motor speed is 592 pps.
4. Deceleration mode C: Used when the CR motor speed is 397 pps.

Table 2.17 Data of decelerate time

Mode	A	B	C
tD1	1.72	1.72	2.56
tD2	1.72	1.72	2.56
tD3	1.72	1.72	2.56
tD4	1.72	1.72	2.56
tD5	1.76	1.76	2.56
tD6	1.80	1.80	2.56
tC7	1.84	1.84	2.60
tD8	1.88	1.88	2.64
tD9	1.96	1.92	2.68
tD10	2.08	1.96	1.96
tD11	2.32	2.04	2.84
tD12	2.52	2.20	2.92
tD13	2.88	2.36	3.12
tD14	3.28	2.60	3.36
tD15	3.76	2.96	3.76
tD16	4.40	3.40	4.40
tD17	5.28	4.08	5.48

Unit: ms

*1

Mode

1163PPS = Draft Pica ESC * 20H
 769PPS = Draft Elite ESC * 26H
 592PPS = Draft Condensed ESC * 21H
 397PPS = LQ ESC * 27H

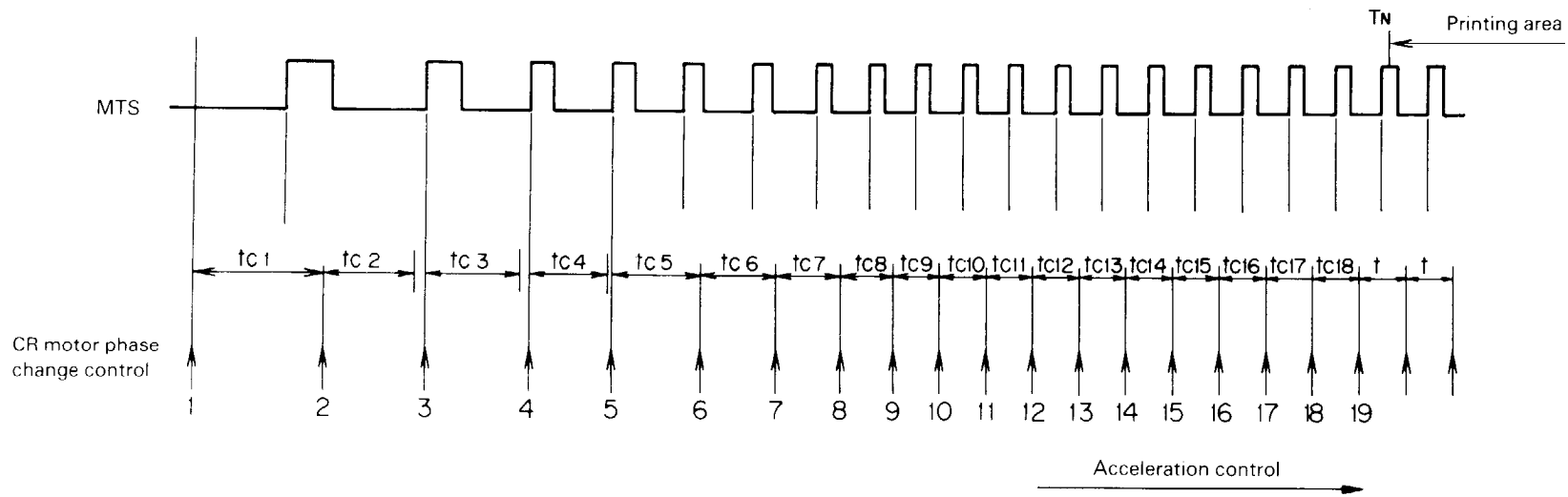


Fig. 2.28 Acceleration and printing control from position other than home position

2-31

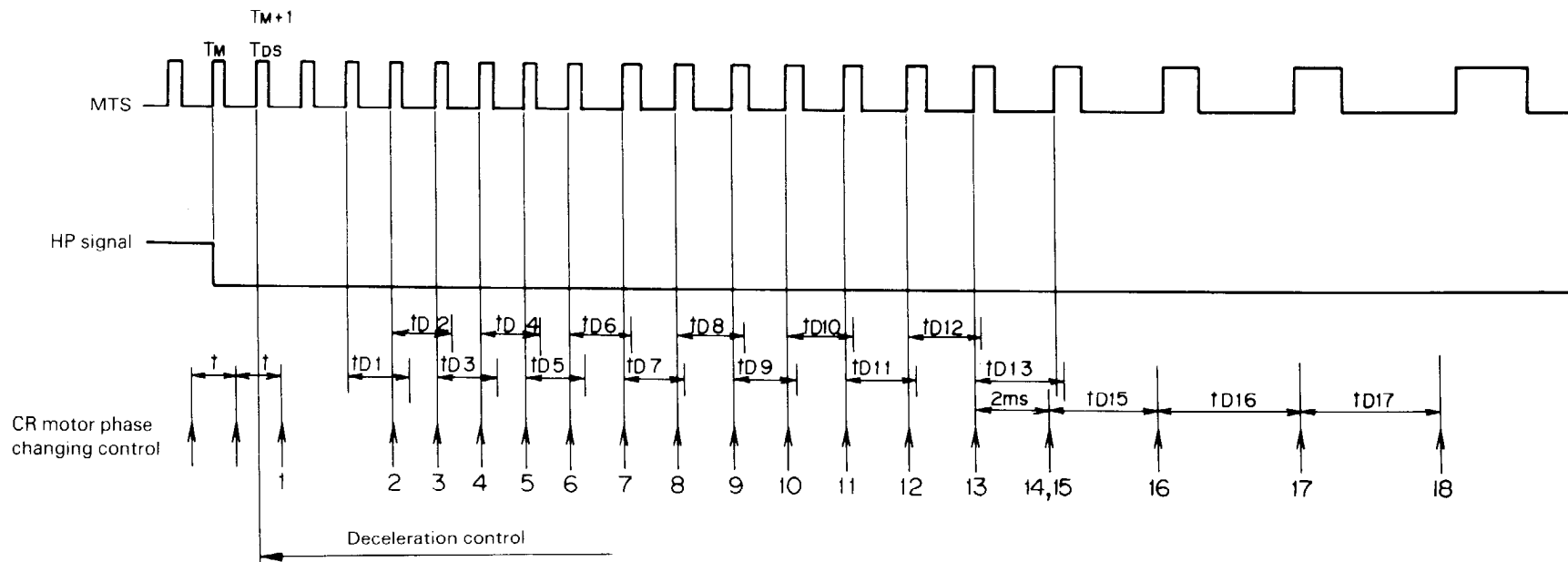


Fig. 2.29 Deceleration and stop at home position (In case of 1163,769 pps)

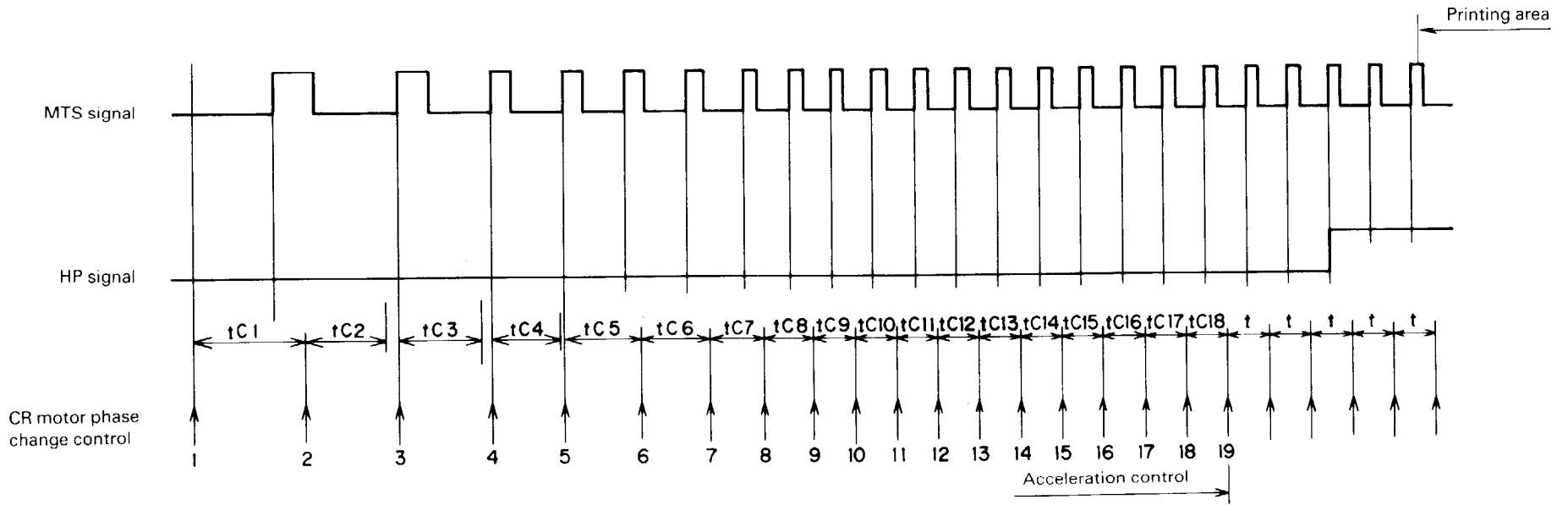


Fig. 2.30 Acceleration and printing control from position other than home position

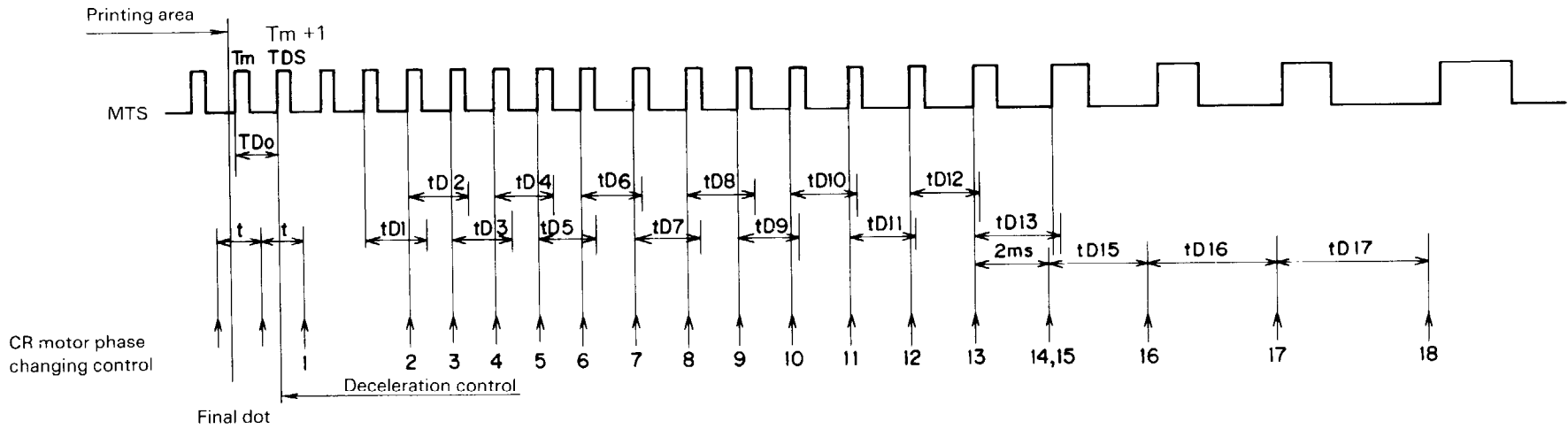


Fig. 2.31 Deceleration and stop at home position (In case of 1163, 769 pps)

(c) Home Position Seek

Movement of the carriage to home position at printer power on is called the home position (HP) seek. The CR motor speeds during the home position seek are all in the 1163 pps mode. The following flow chart exemplifies sequence of HP operational events.

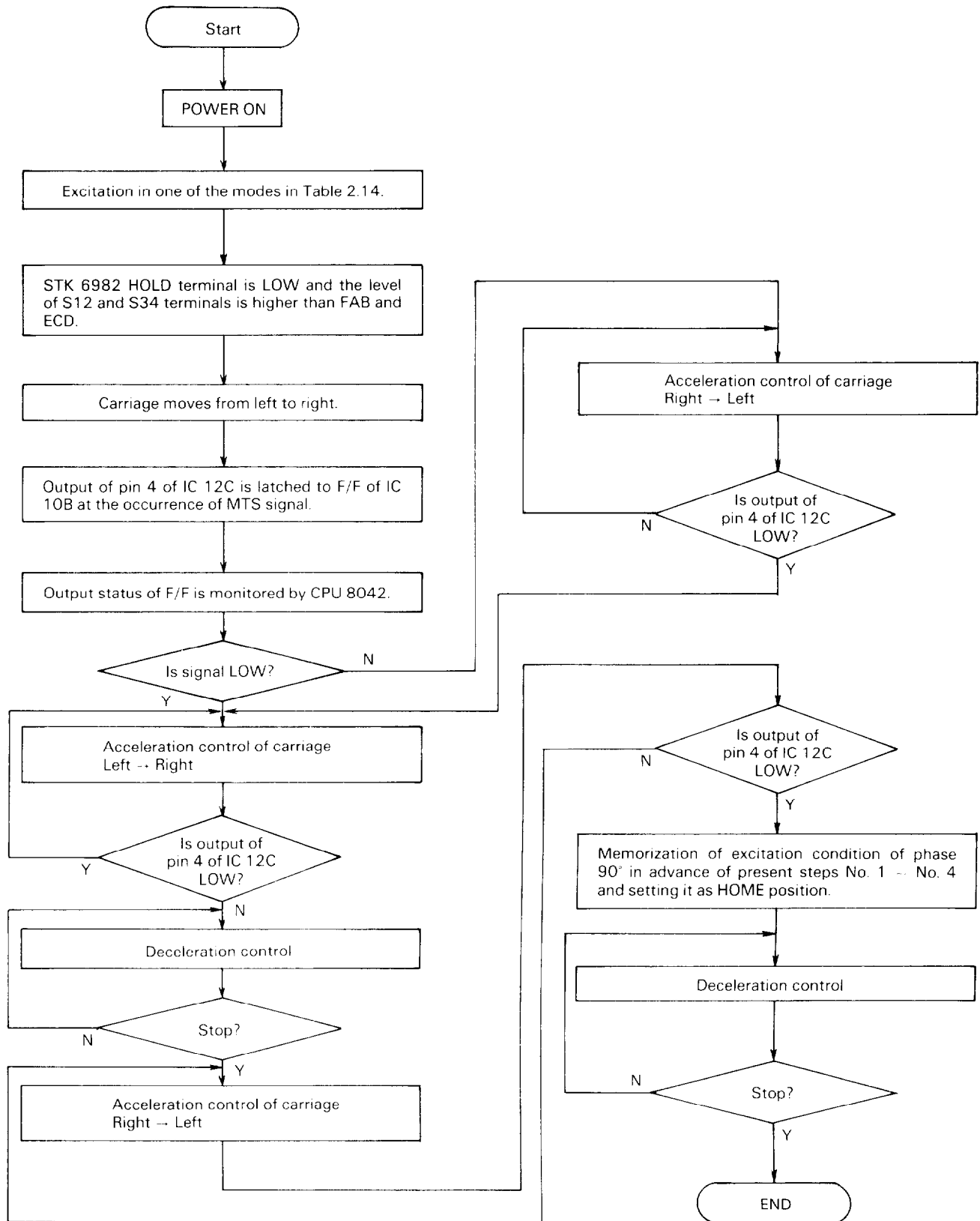


Fig. 2.32 Flow chart of home position seek

(d) Acceleration and printing control from home position:

- ① By the control of a) and b) of 12), the carriage is moved from left to right (column 1 to column 80). In this case, reading to recognize the HP signal is done only in the excitation condition memorized in v) of d). Accordingly the HP signal read timing is every four MTSs.
- ② The print occurs during MTS and thereafter following the MTS where the HIGH of the HP signal is recognized. The printing occurs during maximum of MTS 816 pulses (DTS2448 pulses).

(e) Deceleration stop at positions other than home position:

Deceleration control is started from the next MTS ($T_m + 1 = T$) after the printing of the last dot on the line (MTS immediately after this if T_m). It is stopped after 18 times of phase switching.

(f) Acceleration and printing control from positions other than home position:

- ① By the control of a) and b) of 12), the carriage is moved in a chosen direction.
- ② The printing area is the 19th MTS (T_N) and thereafter.

(g) Deceleration and stop at home position

The HP signal is recognized at every MTS during the shift of the carriage from right to left (column 136 to column 1), deceleration is started from the next MTS ($T_M + 1$) of the MTS (T_M) where the change of HIGH to LOW of HP signal is recognized, and the CR motor is stopped after 18 phase switches.

(h) Setting of speed control terminals

In each control mode the terminals of 8042 (P23 and P24) in the Fig. 2.26 must be set as follows:

Table 2.18

	1163,769 pps	592,397 pps
8042 (P23)	H	L
8042 (P24)	L	H

2.4.5 LF motor control circuit (Fig. 2.34)

The control signal of the 4-phase excitation LF motor (Fig. 2.33) is output from CPU 8041 A on the main circuit board. This signal is sent to IA to ID inputs of the transistor array HA1 3007. With the input at HIGH Level, the inside transistor turns on, forming a closed circuit of power supply (+24V): LF motor, diode, HA1 3007, GND, and the current flows through the coil of the LF motor. The LF motor is thus driven with the voltage-applied phase switched by turning the transistor on and off inside HA1 3007 by the input signal IA to ID.

The operation mode or the non-operation mode can be selected by the output of P27 of CPU 8041 A.

With this output at HIGH, transistor 029 is off and +5V is supplied to LFCOM via resistance R4 and diode D31, putting the LF motor in the non-operation mode. With the output of P27 at LOW, on the other hand, transistor Q29 is on and Vp (+24V) is supplied to LFCOM via D30, putting the LF motor in the operation mode.

Basically, the belt motor is driven by the 2-2 phase excitation system

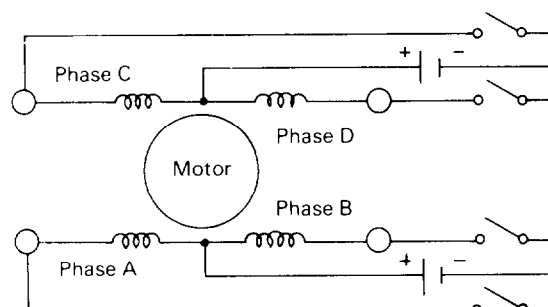


Fig. 2.33 LF motor circuit

Table 2.19 Step motor sequence

Step	Phase A	Phase B	Phase C	Phase D
1	ON	OFF	OFF	ON
2	ON	OFF	ON	OFF
3	OFF	ON	ON	OFF
4	OFF	ON	OFF	ON

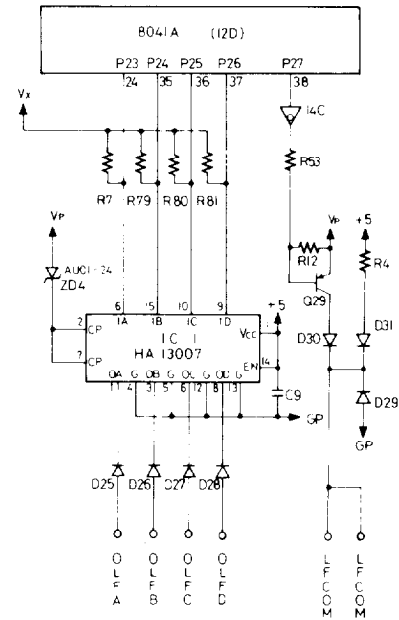


Fig. 2.34 LF motor drive circuit

(1) Motor bias voltage

The bias voltage for the motor is of two types. One for operation use and the other for non-operation use

Table 2.20 Motor bias voltage

Mode	Voltage	Use
Operation	+24V ± 10%	Driving of motor
Non-operation	+5V	Holding bias

(2) Paper feed step motor driven signal timing

Fig. 2.31 shows the time chart for control of the paper feed step motor. The control method is a ramp-up and ramp-down control. The time settings for this control are as shown in Table 2.21.

This control, however, is not performed when the amount of paper feed is five steps or less. The time setting at this time is constant speed drive of 4.2 ms per step.

Table 2.21 Ramp up time settings

Step No.	Time Setting
tC1	4.2 ms
tC2	3.7 ms
t (constant speed)	3.3 ms

The time accuracy is $\begin{matrix} +300 \\ -50 \end{matrix}$ s.

(3) Paper feed pitch

4.23 mm (1/6")/30 pulses

(equivalent to 0.141 mm per pulse)

(4) Paper feed time

3.3 ms/0.141 mm

100 ms/4.23 mm (with continuous paper feed)

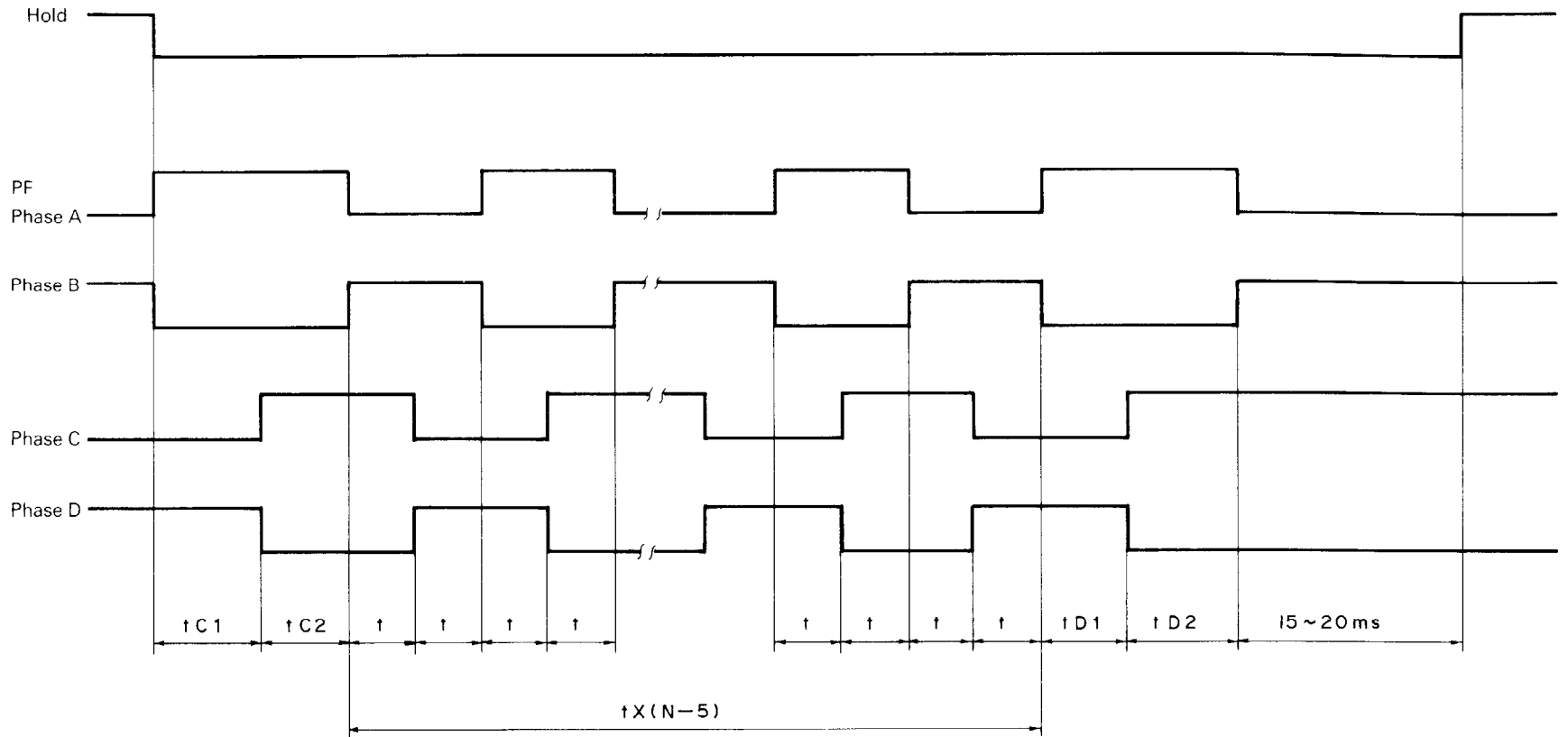


Fig. 2.35 Paper feed timing chart (In case of N pulse paper feed, $N > 5$)

2.4.6 Head driver circuit (Fig. 2.36)

(1) Solenoid driving control

The head has 24 coils and +24V is always supplied to one end of each of the coils. To effect printing with the coils powered, it is necessary to switch on the driver transistors Q1 to Q24 and bring the voltage at one end of the relevant coils to the GND (Fig. 2.32).

A sample sequence is as follows.

Print data put on the data bus are output to each port by a total of five control signals, namely, the A0 and A1 signals from the main CPU Z80A, the control signal from Z80A, the RD and WR signals from the gate array uPB6101-009, producing various timing signals used inside the LQ-1 500, and the chip select signal from the decoder LS138. The output data is input to the transistor array and produces an open collector output and is pulled up to Vx by the block resistance RM1 and RM2.

With the port output of 8255AC-5 going LOW, the out terminal of μ PA79C is internally disconnected from the ground and assumes an Open state.

With the port output of 8255AC5 HIGH, the output terminal of μ PA79C is internally connected to ground. The driving pulse width is determined by the output of pin 11 of IC 10C. When this output is LOW, Q1 is on and the power supply Vx is applied to the base as a pulse to turn on Vcc of μ PS79C and the driven transistor through Q1. Thus the power is supplied to the solenoid and the head pin is driven.

After the lapse of driving time, as shown in Fig. 2.32, the output of pin 11 of IC 10C goes HIGH, Q1 turns off and the supply of Vx stops. The driver transistor 2SD1 392 then turns off to stop the solenoid drive.

When the output of pin 11 of IC 10C goes HIGH, the output of pin 8 goes HIGH simultaneously and by turning Q4 on, the base charge of the driver transistor is released to the ground through block resistances RM1, RM2, R2 and Q4. This realizes a high-speed switching of the driver transistor.

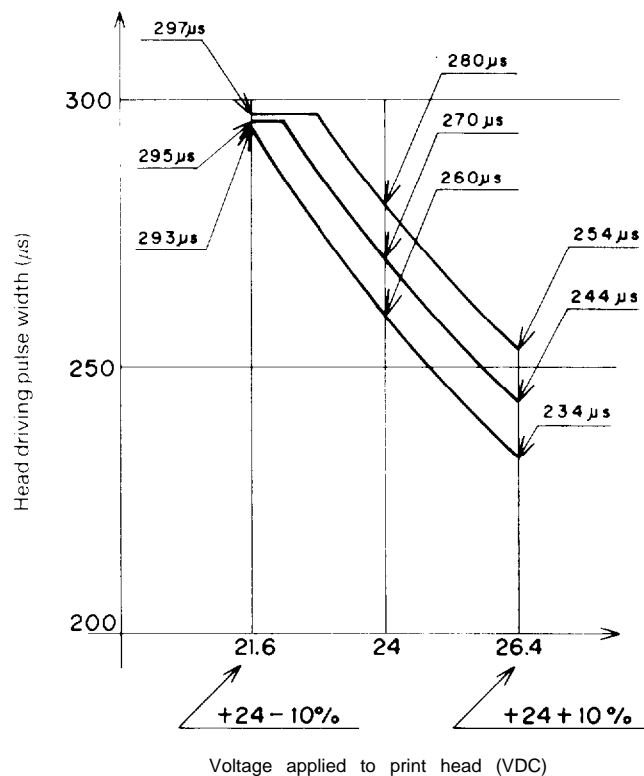


Fig. 2.36 Applied head voltage and driving time

(2) Counterelectromotive force absorbing circuit

As the power supply to the solenoid is switched on and off at high speed, counterelectromotive force is produced in the coil. So that the driver transistor is not adversely affected, a diode and a diode array are provided to each driver transistor (points A, B), and a transistor, resistance, zener diode and electrolytic capacitor (D19, Q27, R6, ZD3, C7) are provided for every 8 driver transistors by wired OR as shown in Fig. 2.37.

As the counterelectromotive force becomes about 44V at point D in the figure, the current flows into the base of Q27 through R6 and ZD3. Then Q27 turns on and the voltage beyond it is fed back to the power supply V_p via 027.

(3) Protective Circuit

The Voltage at point C in Fig. 2.37 is at GND level during the solenoid drive and +24V during the non-drive period. Because of the zener diode ZD3 provided, the current does not flow through the zener diode during the drive. And the output of pin 15 of 15C becomes open and is pulled up to +5V by R23. During the non-drive time, the current flows through the zener diode and the output terminal of pin 15 of 15C is internally connected with ground. The output of pin 2 of 14C on the other hand is internally connected to ground during the drive sequence and is pulled up to +5V during the non-drive period.

The output of pin 15 of IC 15C and the output of pin 2 of 14C are in wired CR. Consequently, as long as a normal power is supplied to the solenoid, point E in Fig. 2.37 is always connected to ground. Because voltage V_x is applied to the base of Q2, Q2 remains OFF.

However, if power is continuously supplied due to failure of the driver transistor, point E in Fig. 2.37 goes HIGH and the base of Q2 lowers to GND. Hence, Q2 turns on, V_x is sent as PSCUT to the power supply circuit, and the power supply circuit, receiving this signal, stops the power supply.

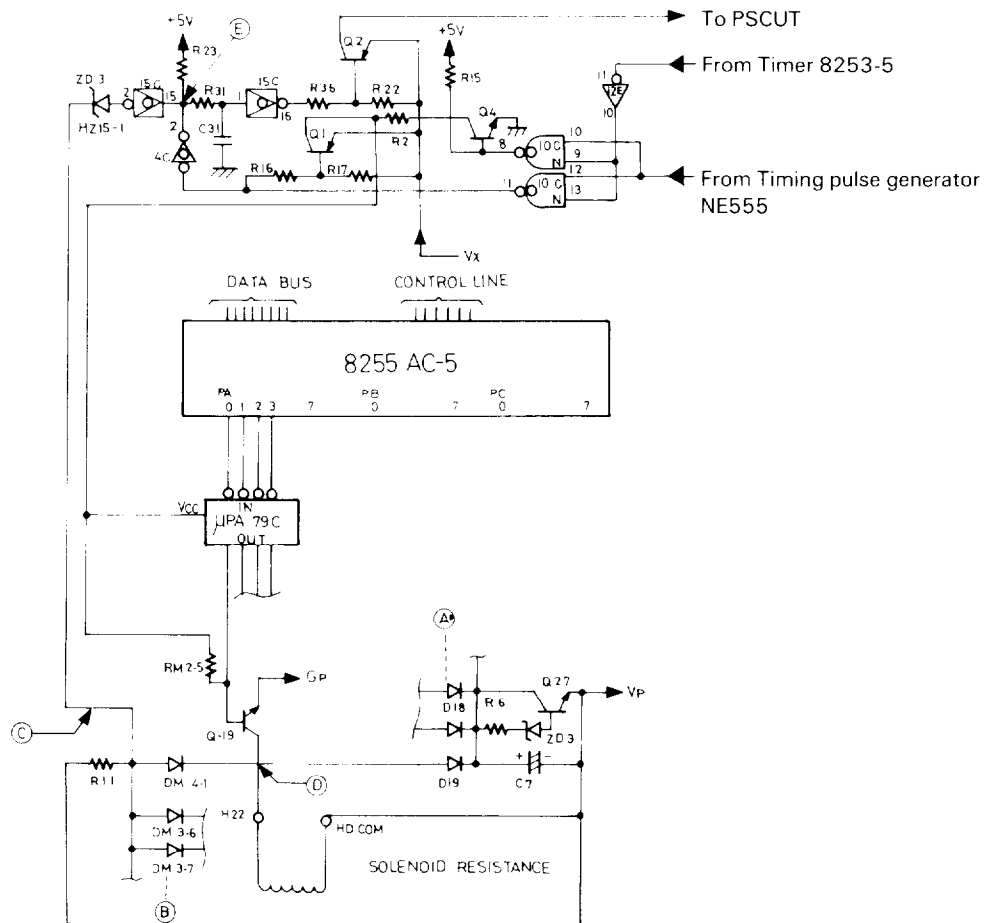


Fig. 2.37 Head driver circuit

(4) Driver circuit waveform

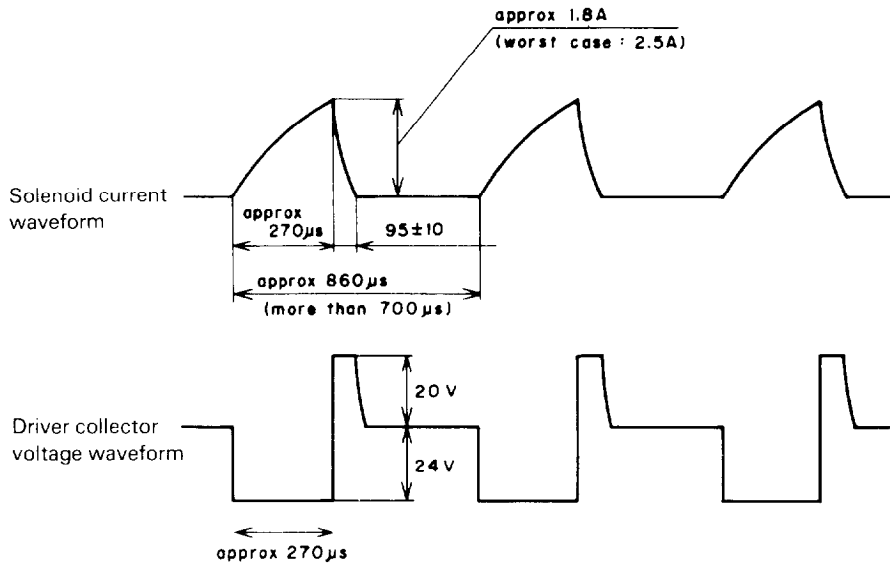


Fig. 2.38 Driver current waveform

2.4.7 Auto sheet load circuit

The auto sheet load circuit sets the paper when the sheet load switch is pressed. The operation consists of the control of the paper hold release lever and the control of the paper feed motor. Refer to 2.4.5 for the control of the paper feed motor. The CPU 8041 (12D) first checks the OFF-LINE condition when sheet load switch on the control panel is pressed. Then, if the printer is OFF-LINE, the 8041 determines whether paper is set in position. When paper is present, the output of P21 of 8041 goes LOW and the output of pin 10 of IC 15C goes off. Since it is pulled up to 5V by R19, Q30 turns on, the solenoid is driven, and the paper hold lever is released.

In this state, the PF motor is driven at 510 pulses to execute paper feeding. On completion of paper feed, CPU 8041 brings P21 to high level. Since pin 10 of IC 15C is internally connected to ground, Q30 turns off, and the base lowers to ground. The solenoid drive is stopped and the paper hold lever turns to the original position. By this control the printing start position is set to about 21 mm from the paper end (print position of head wire 12). And it is about 19.5 mm at the top of character

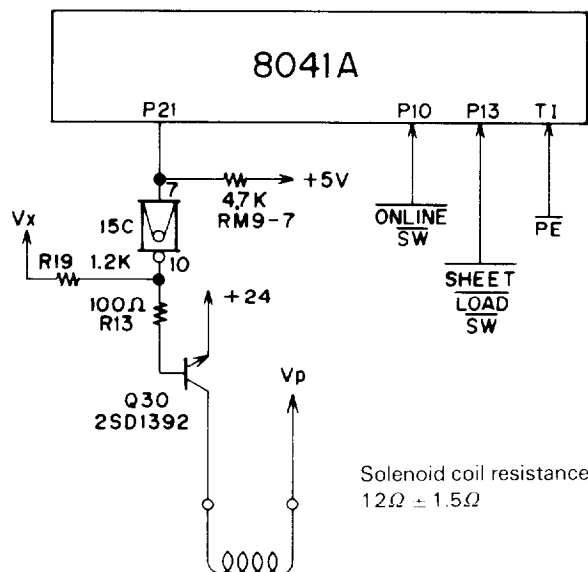


Fig. 2.39 Auto sheet load circuit

2.4.8 Other function

Logical seeking (Fig. 2.40)

The logical seeking maximizes operation speed of the bidirectional printer. It does away with the necessity to start printing from the left end (home position) after each line of printing, but permits printing from any position after a line feed.

- When the power switch is turned on, the head carriage, regardless of its position, returns to the left end, home position in an action of ① to ②.
- Upon receiving print data "EPSON" for a line, the printing is performed in an action of ③ to ⑤ with the head carriage moving to position A.
- The CPU, receiving the next data, analyzes it and determines the acceleration start position of the carriage.
- In an action of ⑥ to ⑦, the carriage is moved to position B. Then it goes through acceleration, printing and deceleration.
- In an action of ⑪ to ⑫, acceleration and printing are performed. Then the carriage returns to the home position because in this case the stop position is considered equivalent to the reset position.

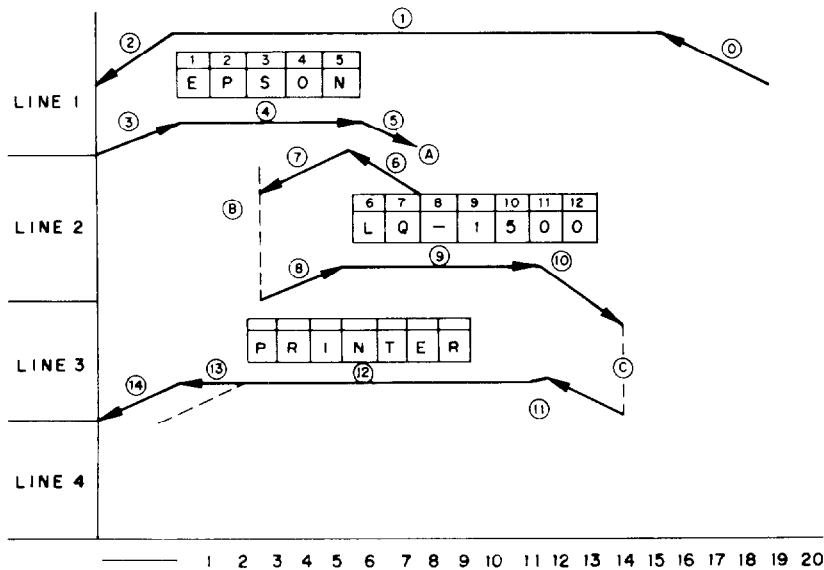


Fig. 2.40 Logical seeking

- 0 ~ 2 Reverse action at power "on".
- 3 ~ 5 Printing of 1st line.
- 6 ~ 7 Logical seeking.
- 8 ~ 10..... Printing of 2nd line.
- 11 ~ 12..... Printing of 3rd line.
- 13 ~ 14..... Logical seeking (The carriage returns to the home position when the stop position of a slow-down sequence is considered equivalent to the reset position.)

Condition	Action No.	Action
A	0, 6, 11	Speed-up (Reverse)
B	1, 12	Reverse
C	2, 7, 14	Slow-down (Reverse)
D	3, 8	Speed-up (Forward)
E	4, 9	Forward
F	5, 10	Slow-down (Forward)

2.5 Printer Mechanism (Model-3660)

The Model-3660 printer mechanism features a 24-pin print head and incorporates all of the sophisticated technology of previously produced EPSON printers.

Operation of the 24-pin print head is supported by the carriage components, including the timing belt, ribbon driving gears, and the carriage motor; the paper feed mechanism, including the platen sprocket assemblies and paper feed motor; and the sensors, which communicate the disposition of the print head and the paper supply at any given time. The printer mechanism is illustrated in Fig. 2.41.

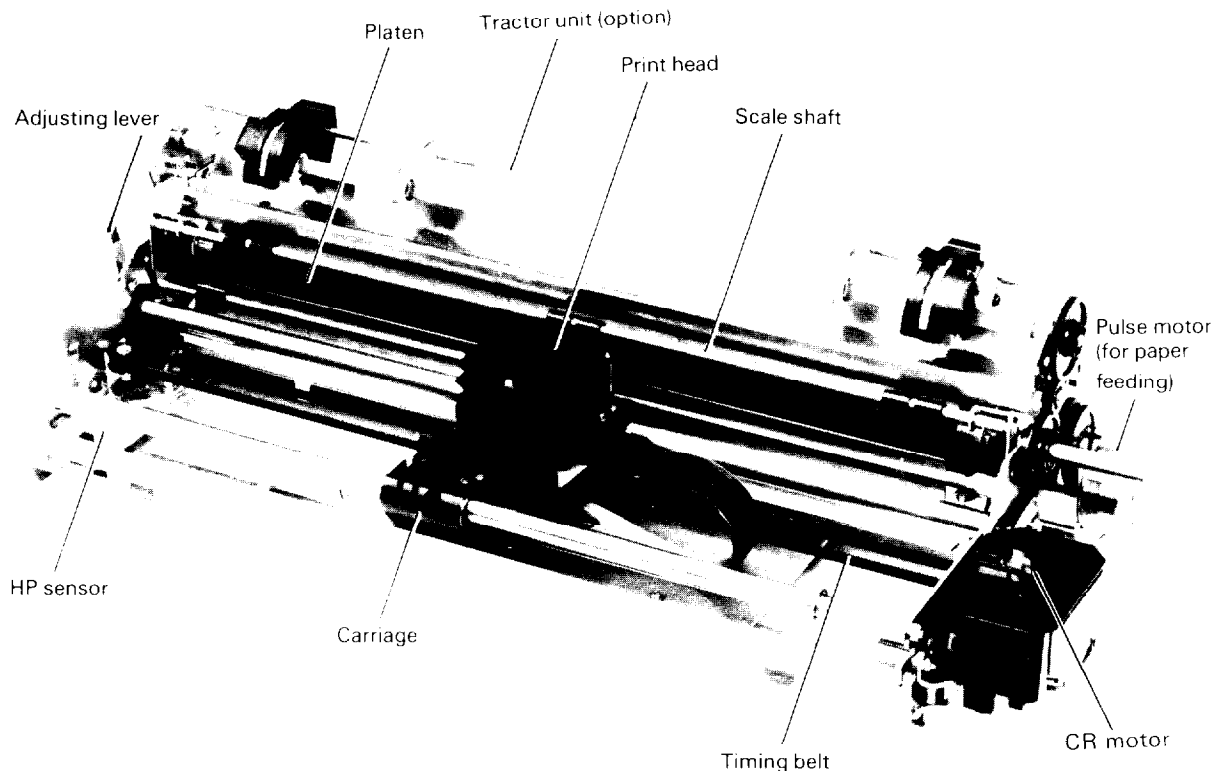


Fig. 2.41 Appearance of the printer

2.5.1 Operation

2.5.1.1 Sensor mechanism (Signal generating mechanism of Model-3660)

The sensor mechanism is composed of an HP (home positron) sensor, an MTS/DTS sensor, a PE (paper end) sensor and a print head temperature sensor.

- The purpose of the HP sensor is to determine the home position of the carriage. The sensor generates a reference signal for the printing position.
- The MTS/DTS sensor detects the carriage speed and print timing.
- The PE sensor detects the presence or absence of paper.
- The print head temperature sensor detects the internal temperature of the print head. The sensor outputs a signal when the print head reaches temperature levels which could damage components.

1) HP (home position) sensor

The HP sensor consists of an HP sensor board and a sensor plate located at the bottom of carriage. While the sensor plate intercepts the optical axis of the photocoupler, a HIGH signal is emitted (open collector output).

2) MTS/DTS sensor (print timing signal sensor)

The MTS/DTS sensor consists of an MTS/DTS sensor board and a sensor plate located on the carriage motor shaft. When the slit of the sensor plate comes to the predetermined position, an LOW signal is given (open collector output).

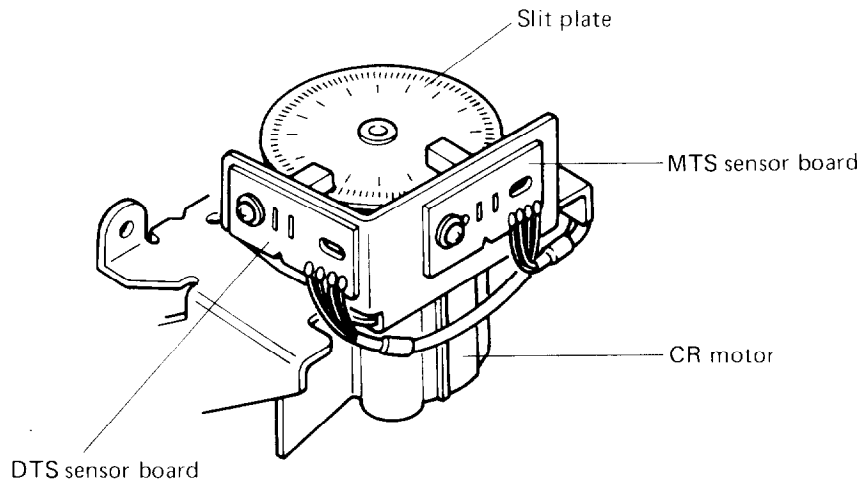


Fig. 2.42 MTS/DTS sensor

3) PE (paper end) sensor

The PE sensor consists of a Hall IC mounted on the PE sensor board and a permanent magnet mounted on the PE sensor lever. When the printer is out of paper, the magnet touches the Hall IC and generate a signal.

4) Print head temperature sensor

Two thermistors are built into the print head to detect excessive temperature gains. Their resistance value aids in maintaining component compatible operating temperatures.

2.5.1.2 Print head assembly

The print head unit mounted on the carriage is moved right and left on the carriage shafts A and B by the operation of the timing belt. This belt is driven by the timing belt motor assembly through the belt driving pulley and belt driven pulley.

1) Carriage assembly (Fig. 2.43)

The carriage assembly is moved by the timing belt which is driven by the four phase carriage motor. Each motor phase produces a movement of the carriage. As the timing belt motor runs, the DTS signal is generated, and current is also fed through the head driving coil, causing the dot wires to fire.

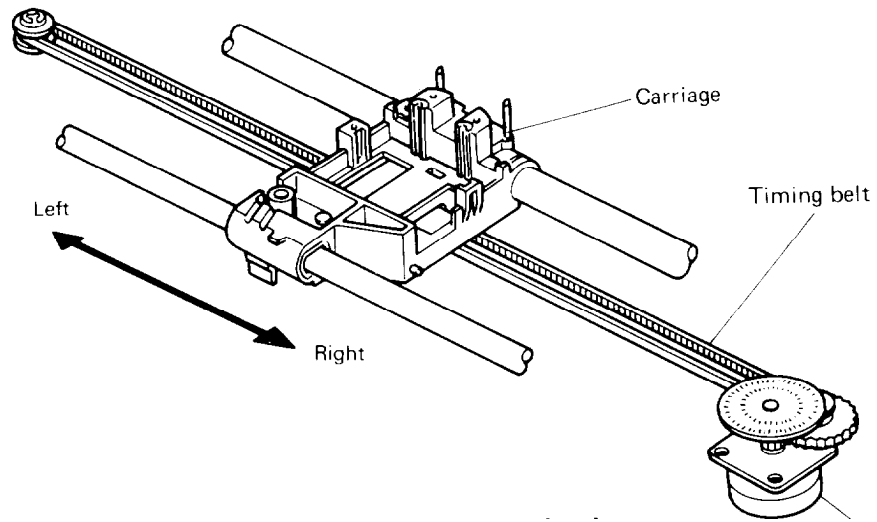


Fig. 2.43 Carriage mechanism

2) Operation of print head unit (Fig. 2.44)

The movement of a dot wire in printing a dot is as follows:

- ① With the current flowing through the head driving coil, the actuator plate is attracted to the iron core. At this time, the dot wire, which is engaged with the actuator plate, flies out against the platen assembly.
- ② The dot wire thus pushed out strikes at the platen assembly and prints a dot on the paper through the ribbon
- ③ On completion of the supply of current to the head driving coil, the actuator plate is caused to return to its original position by the action of the spring. By the impact energy and the force of the wire return spring, the dot wire is brought back to the original position to engage with the actuator plate and held in readiness.

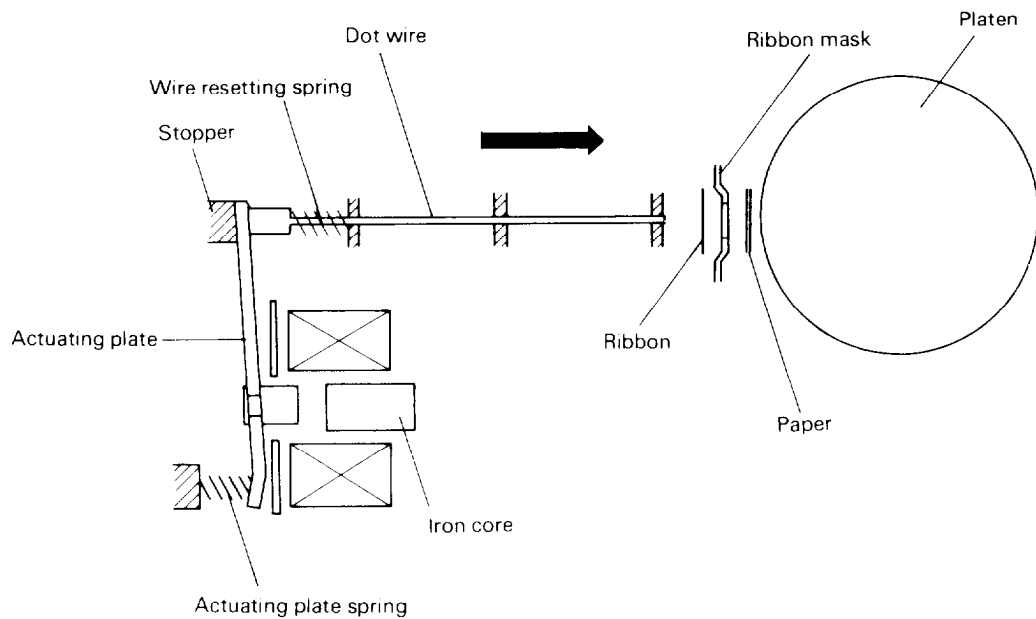


Fig. 2.44 Print mechanism

3) Correspondence between dot wires and FPC terminals

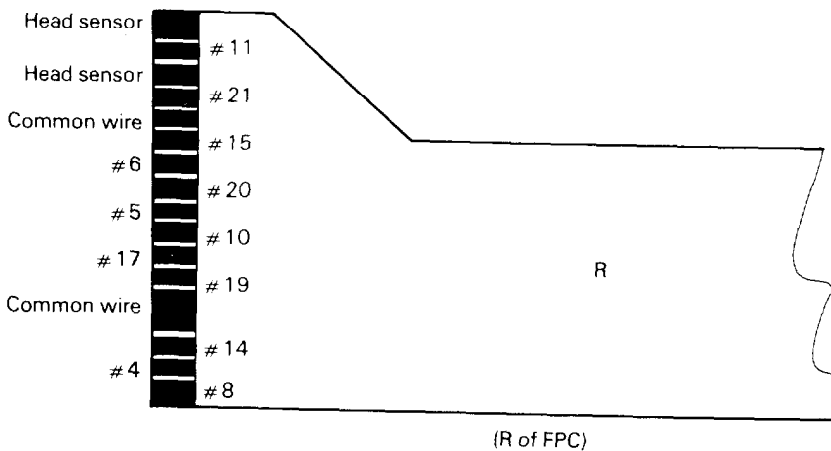
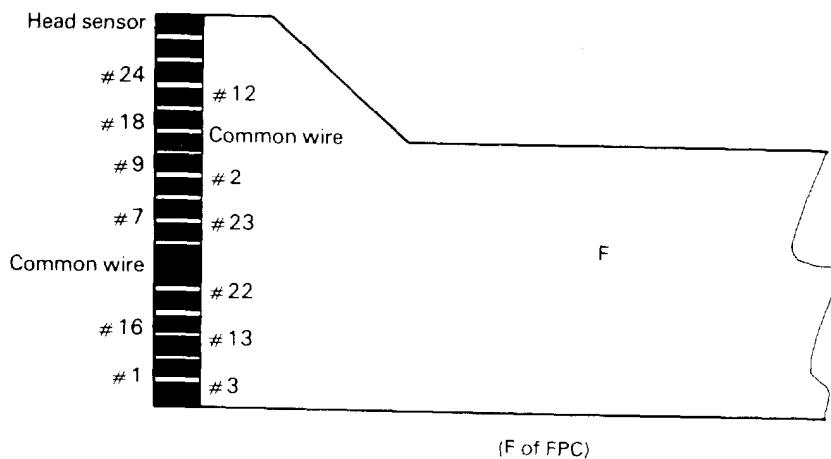
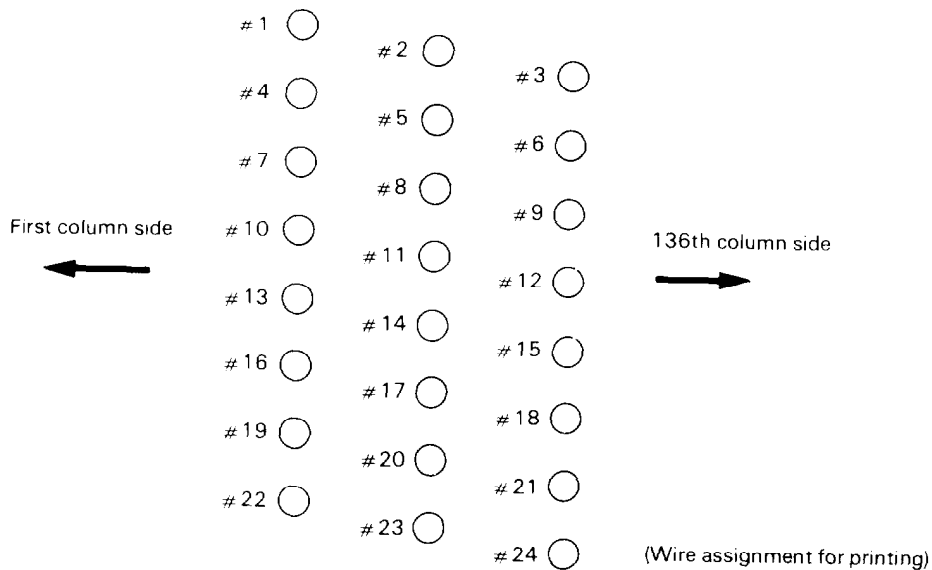


Fig. 2.45 Printhead connector

2.5.1.3 Paper feeding mechanism

The paper feeding mechanism of the printer comprises two systems: a friction feed system to be used for cut sheet and a tractor feed system to be used for continuous business form 4 - 16 inches in width. Each of the two systems have functions such as ordinary feeding and quick feeding. The printer is also equipped with an auto loading mechanism for setting cut sheet automatically for printing.

1) Friction feed system (for cut sheet) (Fig. 2.47)

The paper is held between the platen, the paper feeding rollers and the paper holding rollers. When the pulse motor rotates, the gears constituting a paper feeding gear train are driven in the directions of arrows, respectively. Consequently, the paper is frictionally fed by the platen, paper holding rollers and paper feeding rollers in the direction of the arrow. The paper holding rollers and paper feeding rollers are pressing the paper against the platen by the action of springs.

The paper can be set free by operating the release lever.

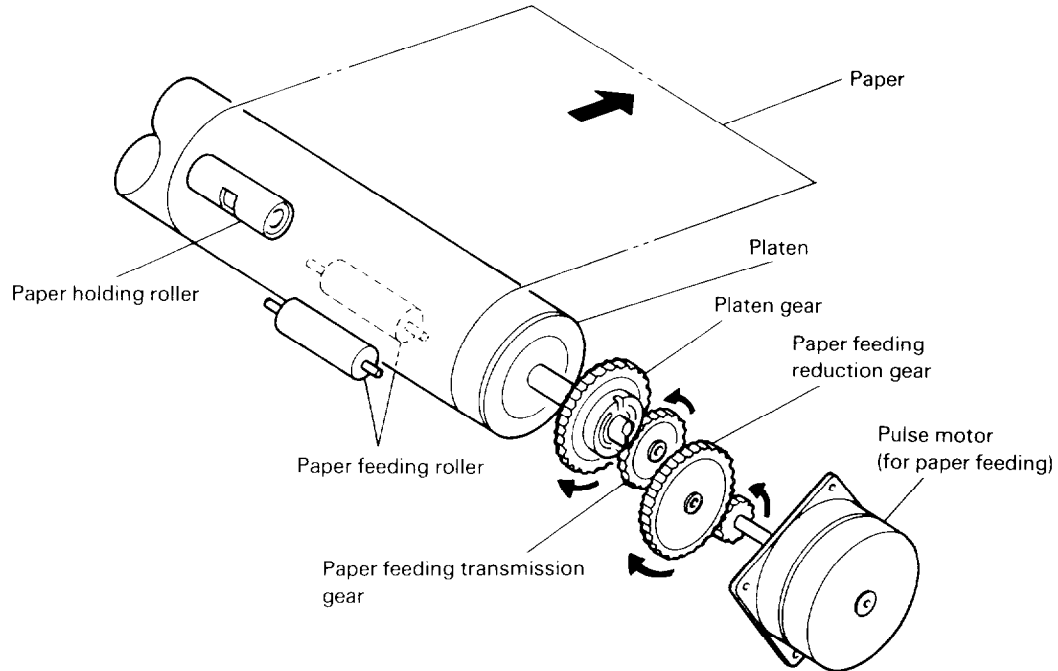


Fig. 2.46 Friction feed mechanism

2) Tractor feed system (for continuous business from 4 - 16 inches in width)

The paper is held on sprocket wheels, some of the sprocket pins being engaged in holes in the paper. When the pulse motor rotates, the gears in the paper feeding gear train are driven in the directions of arrows, respectively. Consequently, the paper is driven by the sprocket wheels in the direction of the arrow.

When the tractor feed system is used, the paper feeding rollers are held apart from the platen by the action of the release lever.

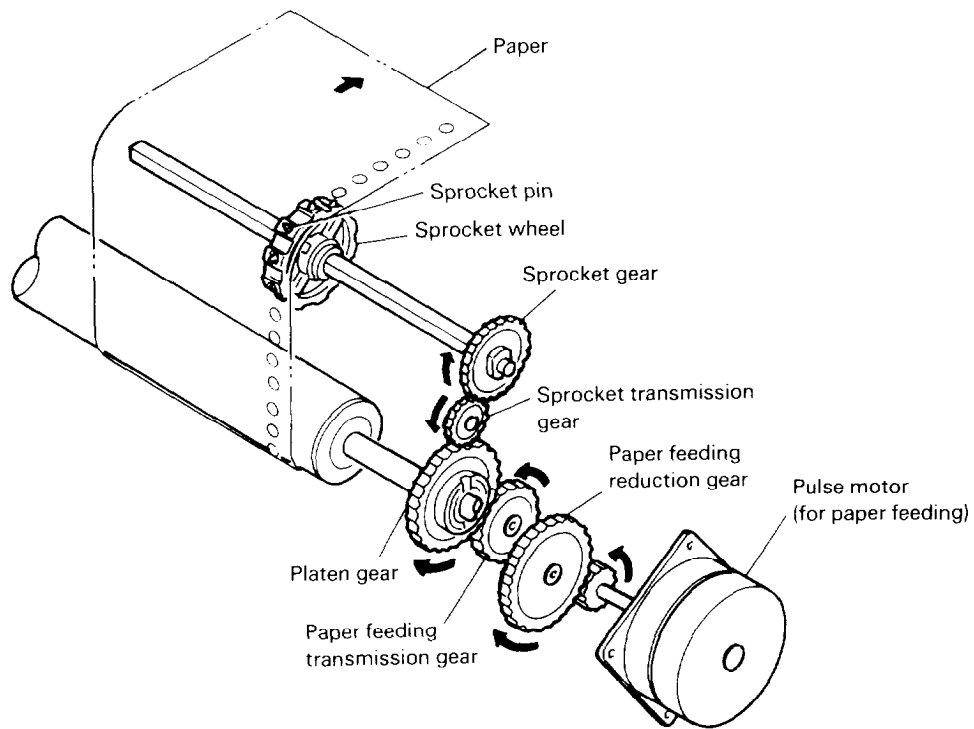


Fig. 2.47 Tractor (sprocket) feed mechanism

3) Auto loading mechanism

Set a cut sheet between the platen and the paper feeding lever. When the release solenoid is energized, the solenoid shaft, sub paper holding lever and paper holding lever move in the direction of the arrow respectively to disengage the paper holding roller from the platen. At this point, the pulse motor (for paper feeding) is driven to feed the paper as specified. When the release solenoid is deenergized, the solenoid shaft, sub paper holding lever and paper holding lever return to their original positions respectively, causing the cut sheet to be pressed against the platen and set for printing.

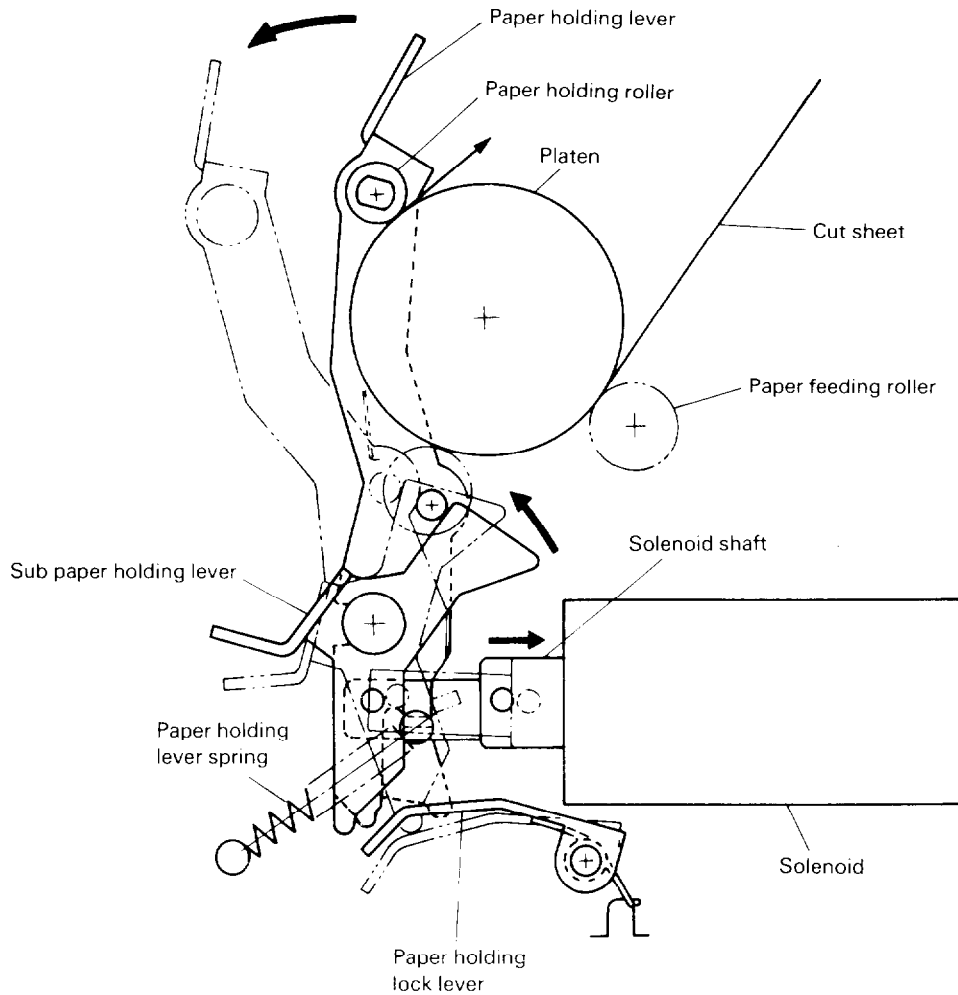


Fig. 2.48 Auto loading mechanism

2.5.1.4 Ribbon feeding mechanism (Fig. 2.49)

The ribbon unit consists of a cassette ribbon and a ribbon feeding mechanism. The ribbon feeding mechanism is set at the bottom of the carriage.

When the carriage moves to right or left, the ribbon driving pulley is turned by the ribbon driving wire wound around it so that the ribbon driving gear always turns counterclockwise in the next gear train.

	Direction of movement of carriage	Gear train
1	Left to right (arrow →)	Ribbon driving pulley → Planetary pinion ① → Planetary pinion ② → Ribbon driving gear
2	Right to left (arrow ⇐)	Ribbon driving pulley → Planetary pinion ① → Planetary pinion ③ → Planetary pinion ④ → Ribbon driving gear

The inked ribbon is housed in the cassette case in an endless state. The inked ribbon between the ribbon feeding roller and the ribbon pressure roller is fed when the ribbon feeding roller set in the ribbon driving gear is turned.

A ribbon braking spring is provided at the exit of the cassette case for preventing the ribbon from losing tension, and a ribbon mask is provided for protecting the paper from being stained by the inked ribbon.

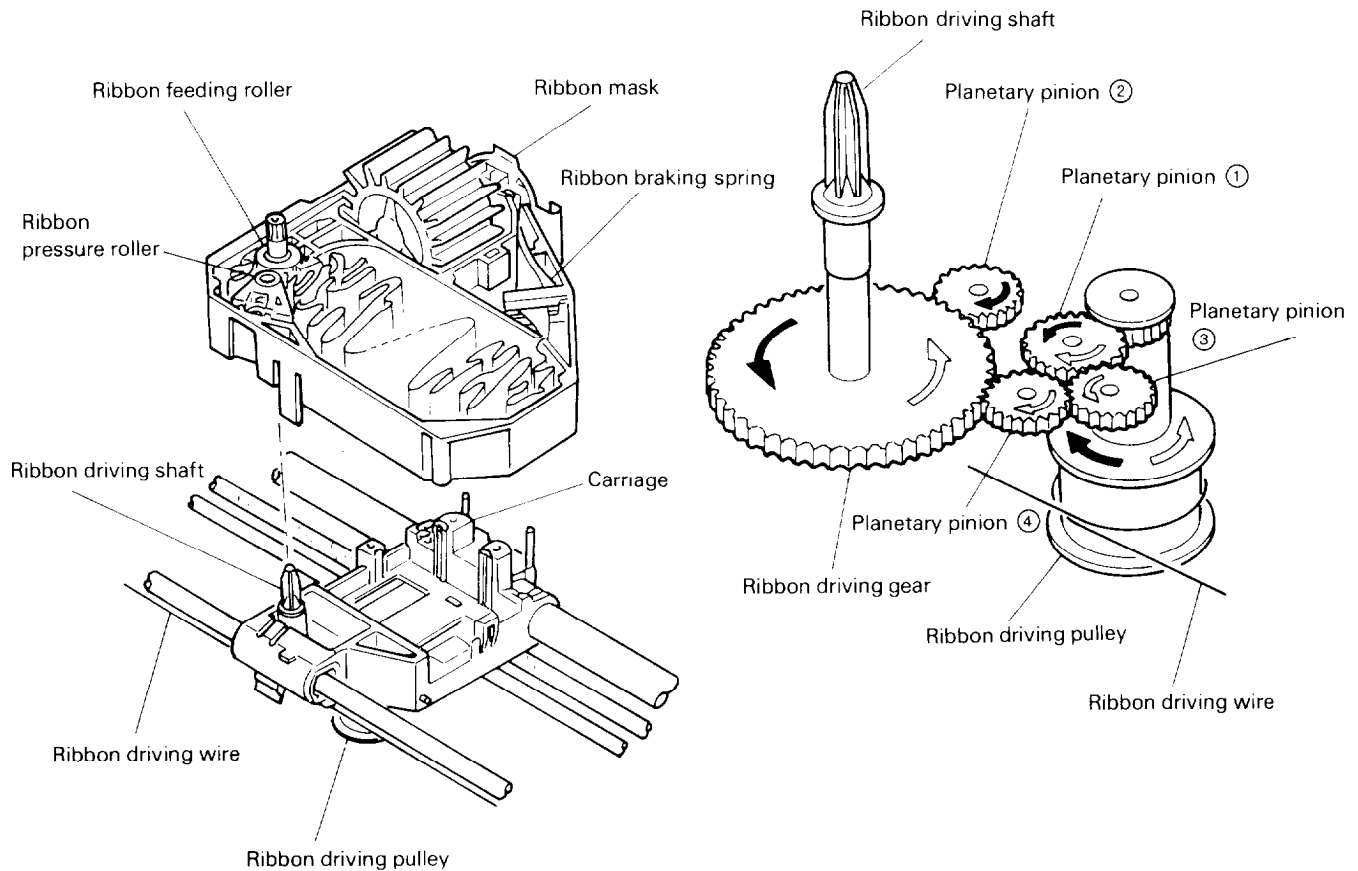


Fig. 2.49 Ribbon feed mechanism

CHAPTER 3

OPTIONAL EQUIPMENT

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3.1 Centronics Compatible Parallel Interface Unit (Cat. No. 7171)

3.1.1 Overview

With the IUPIF interface board, a centronics parallel data from a host computer can be output to and printed dot by the EPSON LQ-1500 terminal printer.

3.1.2 Specification

3.1.2.1 Interface

- (1) Data Transmission : 8-bit parallel
- (2) Synchronization : Externally supplied $\overline{\text{STROBE}}$ pulses
- (3) Handshaking : $\overline{\text{ACKNLG}}$ or $\overline{\text{BUSY}}$
- (4) Logic level : Input data and all interface control signals are TTL compatible.

3.1.2.2 Condition setting on the interface board

These are two DIP switches on the centronics parallel interface board. These switches are set as follows:

(1) DIP switch setting

A. DIP 1

Table 3.1

DIP 1	Function	Setting Options		Factory Setting
		ON	OFF	
1-1	2KB INPUT buffer	Disabled	Enabled	OFF
1-2	Paper-end detector	Disabled	Enabled	OFF
1-3	$\overline{\text{AUTO FEED XT}}$ signal	Fixed	Not fixed	OFF
1-4	NOTE 1 ———	—————	—————	Always OFF

B. DIP 2

Table 3.2

DIP 1	Function	Setting Options		Factory Setting
		ON	OFF	
2-1	International Character			ON
2-2	Selection			ON
2-3	(See Table 3.3)			ON
2-4	Form length	12"	11"	OFF
2-5	1-inch Skip-over perforation	Enabled	Disabled	OFF
2-6	Buzzer Ring	Disabled	Enabled	OFF
2-7	Print Quality	NLQ	DRAFT	OFF
2-8	$\overline{\text{SLCT IN}}$ signal	Fixed	Not fixed	ON

Note 1: With this switch ON, the printer does not perform normal operation.

Table 3.3

2-1	2-2	2-3	Country
ON	ON	ON	U.S.A. (ASCII)
ON	ON	OFF	France
ON	OFF	ON	Germany
ON	OFF	OFF	England
OFF	ON	ON	Denmark
OFF	ON	OFF	Sweden
OFF	OFF	ON	Italy
OFF	OFF	OFF	Spain

3.1.2.3 Pin assignment of interface connector

- A. CN1 : This connector communicates with CN1 of the UXMCL board. (Refer to Table 3.1)
 - B. CN2: Future specification
 - C. CN3: This connector communicates with the host computer.
- (1) Number of pins.....36 pins

Table 3.4 Pin assignment (CN3 of IUPIF)

	Signal Pin No.	Return Pin No.	Signal	Transmitter	Description
Parallel Interface With these signals, use twisted-pair cable and connect "Return" to LOGIC GND. Note: The signals which are active at "LOW" are indicated by a bar above.	1	19	$\overline{\text{STROBE}}$	Host Computer	STROBE pulse for read-in of data, pulse width must be more than 0.5 μs at receiving terminal. The signal level is normally HIGH; read-in of data is performed at the LOW level of this signal.
	2	20	DATA1	Host Computer	These signals represent information of the 1st to 8th bits of parallel data respectively. Each signal is at HIGH level when data is logical 1 and LOW when logical 0.
	3	21	2		
	4	22	3		
	5	23	4		
	6	24	5		
	7	25	6		
	8	26	7		
	9	27	8		
	10	28	ACKNLG	Printer	LOW signal indicates that data has been received and that the printer is ready to accept other data. Approx. 12 μs pulse.

	Signal Pin No.	Return Pin No.	Signal	Transmitter	Description
	11	29	BUSY		A HIGH signal indicates that the printer cannot receive data. A LOW signal indicates that the printer can receive data. The signal becomes HIGH in the following cases: 1. During data entry 2. During printing operation and part of head carrier operation 3. During part of paper feed 4. During printer error status 5. In OFF-LINE state
	12	30	PE	Printer	A HIGH signal indicates that the printer is out of paper.
	13		SLCT	Printer	Pulled up to +5V through 3.3 k Ω resistance
	14		$\overline{\text{AUTO FEEDXT}}$	Host Computer	With this signal being at LOW level the paper is automatically fed one line after printing.
	15		NC		Not used.
	16		GND		LOGIC GND level.
	17		FG		Printer FRAME GND.
	18		NC		Not used.
	19 ~ 30		GND		TWISTED-PAIR RETURN signal GND level.
	31		$\overline{\text{INIT}}$	Host computer	When the level of this signal becomes LOW, the print buffer memory is cleared. The pulse width must be more than 50 μs at the receiving terminal.
	32		$\overline{\text{ERROR}}$	Printer	The level of this signal becomes LOW. When the printer is in the error status: 1. PAPER END state (cancelled by ESC8) 2. Abnormal motor operation 3. OFF-LINE state
	33		GND		Twisted pair return level at ground.
	34		NC		Not used.
	35		+5V	Printer	Pulled up to +5V through 3.3 k Ω resistance
	36		$\overline{\text{SLCTIN}}$	Host Computer	With this signal being at LOW level, the printer is selected.

1. The return side, i.e. a twisted pair return, is connected to the signal ground level. A twisted pair line must also be used for each signal for the interface and to connect the return side. To effectively prevent noise, shield this signal line cable and connect it to the enclosure grounds of the host computer and printer, separately.
2. All interface condition are TTL based. The rise and fall times of each signal shall be less than 0.2 ©sec.
3. For details of the timing of each signal, refer to the timing chart.
4. Fata should be transferred to the printer after checking pulse ACKNLG or when signal BUSY is LOW.
5. Signal AUTO FEED XT can be fixed to LOW when DIP switch SW2-3 is set ON.
6. When ACKNLG and STROBE are connected with the interface connector, DATA1 to 8 are set to an appropriate character code ("1 " at open against GND, "0" at short). A printing test including that for the interface circuit can be executed without external equipment.

3.1.3 Operating principle

3.1.3.1 Data entry

As the interface board (IUPIF) is non-buffered, a 2 K-byte RAM on the main board (UXMCL) can serve as an input (reception) buffer. This option is selectable via DIP switch setting on the interface board.

3.1.3.2 Buffer full/empty control

Table 3.5

DIP 1-1	ON	2 K-byte input (reception) buffer, valid
DIP 1-1	OFF	2 K-byte input (reception) buffer, invalid

(1) When the input buffer is valid

Since signal BUSY is LOW until the 2 K-byte input buffer becomes full, the data from the host computer is entered in the input buffer on the UXMCL board through 8255AC-5.

At the same time, developing the print pattern for one line starts for the 7 K-byte print buffer by Z-80A CPU on board UXMCL. When the input buffer is partly empty, the data is entered, even during printing or line feed. When the input buffer is full, the BUSY signal is HIGH, data entry is prohibited.

(2) When the input buffer is invalid

The data is entered in through Interface 8255AC5 byte by byte. When 2 bytes of data are entered, signal BUSY becomes HIGH to prohibit data entry.

At the same time that the data is entered in the buffer, a print pattern is developed for the print buffer by Z-80A CPU on board UXMCL.

3.1.3.3 Handshaking of the parallel interface

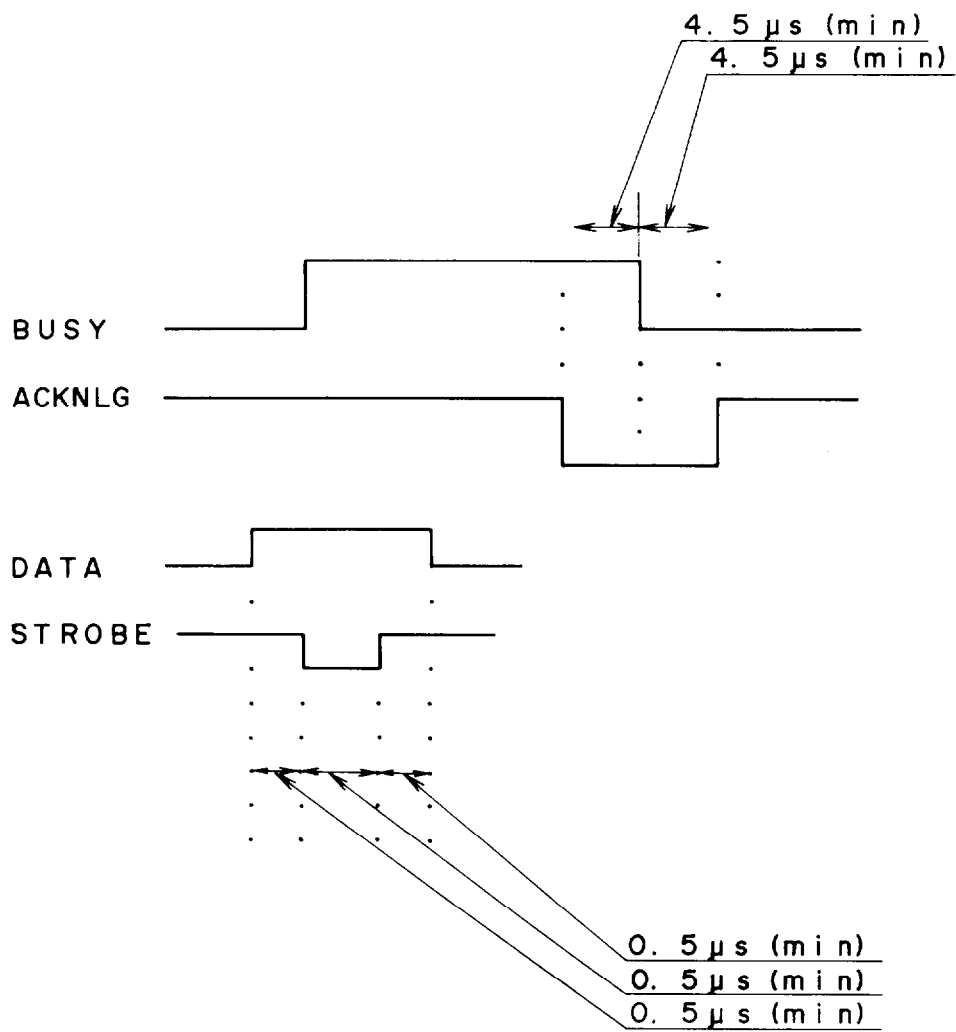


Fig. 3.1 Parallel interface timing

3.1.4 Block diagram

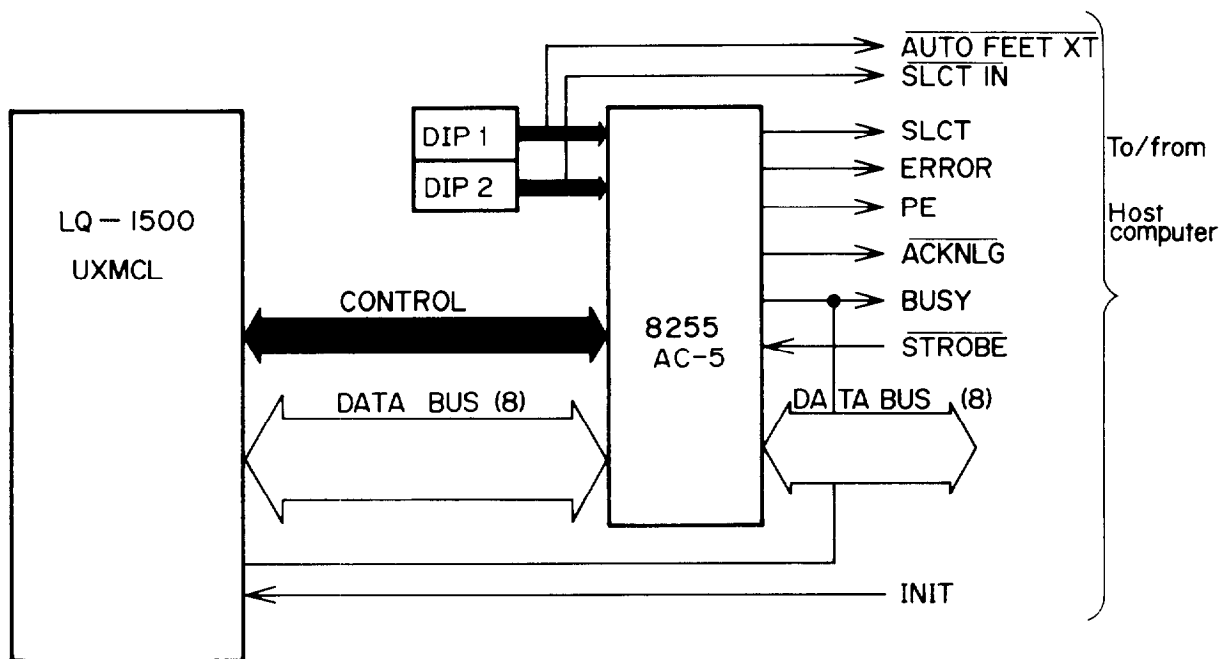
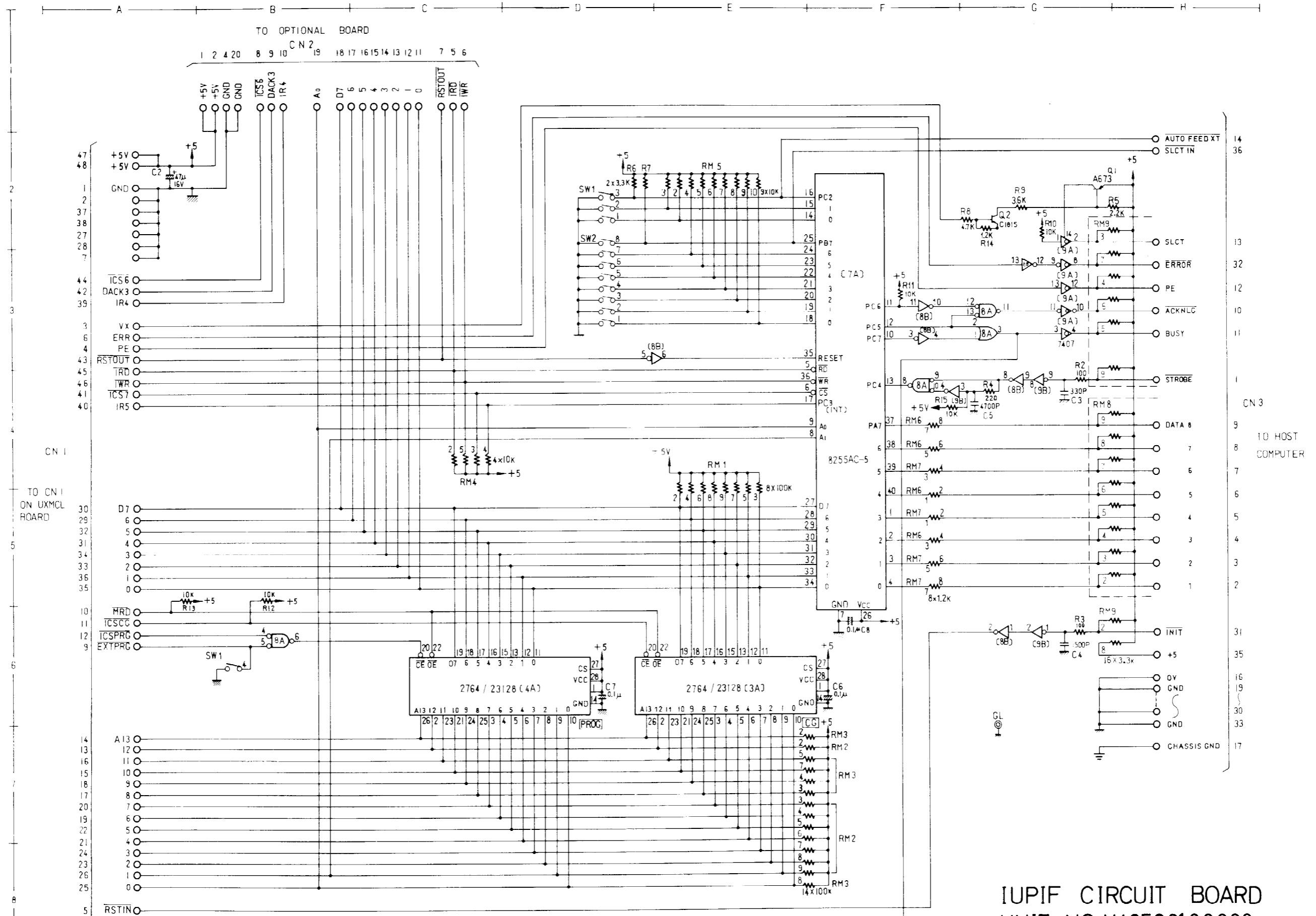


Fig. 3.2 Block diagram

Data is exchanged between the UXMCL and IUPIF boards through the 8255AC-5, a programmable peripheral interface. The data bus from the UXMCL board is connected to 8255AC-5 data pin $D_0 - D_7$. Port B is connected to DIP switches DIP 1 and DIP 2. Ports A and C are used for handshaking with the host computer. As no RAM is incorporated in 8255AC5, interface board IUPIF is non-buffered.

3.1.5 Circuit diagram



IUPIF CIRCUIT BOARD

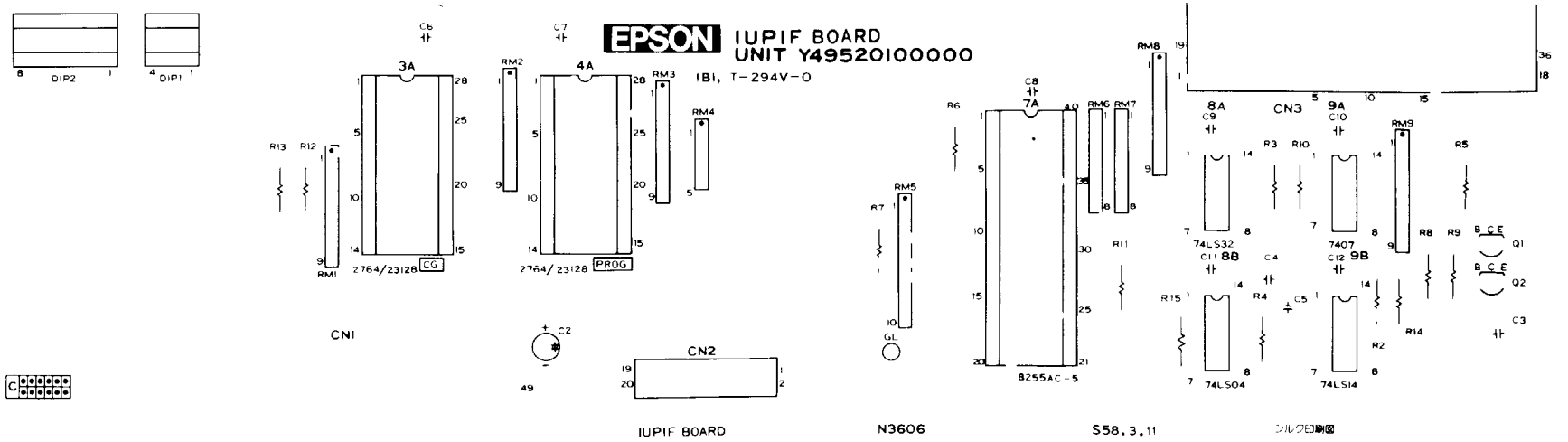


Fig. 3.4 Component layout of IUPIF board

3.2 RS-232C/Current Loop Interface (Cat. No. 7148)

3.2.1 Introduction

The interface is a general-purpose, intelligent, serial interface which enables the data from different computers to be output to the EPSON LQ1500 terminal printer. Board components include a CPU, and a 2 K-byte buffer, which has flag control and X-ON/X-OFF control functions.

Under the interface conditions of RS232C or 20 mA current loop, this interface can be applied to asynchronous serial data transmission systems with a bit rate ranging from 75 to 19,200 BPS under X-ON/X-OFF control or Reverse channel control

3.2.2 Specification

3.2.2.1 Interface

- (1) Synchronization : Asynchronous
- (2) Bit Rate : 75, 110, 135, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600, 19200 (Selectable by DIP switch)
- (3) Word Length
 - (a) Start bit : 1 bit
 - (b) Data bit : 7 or 8 bits (Selectable by DIP switch)
 - (c) Parity bit : Odd or Even or none (Selectable by DIP switch)
 - (d) Stop bit : 1 bit or more
- (4) Input signal Polarity
 - (a) With RS-232C : Mark = Logic "1" (-3V ~ -27V)
Space = Logic "0" (+3V ~ +27V)
 - (b) With current loop : Mark = Logic "1" (current ON)
Space = Logic "0" (current OFF)
- (5) Handshaking
 - (a) With FLAG control

Flag control

Table 3.6

Data X'fer	RS 232C	Current Loop
Enabled	Pin No. 11 (REV) and pin No. 20 (DTR) SPACE state.	Impedance between pin No. 17 (TTY-TXD) and pin No. 24 (TTY-TXDR) LOW state.
Disabled	Pin No. 11 (REV) and pin No. 20 (DTR) MARK state.	Impedance between pin No. 17 (TTY-TXD) and pin No. 24 (TTY-TXDR) HIGH state.

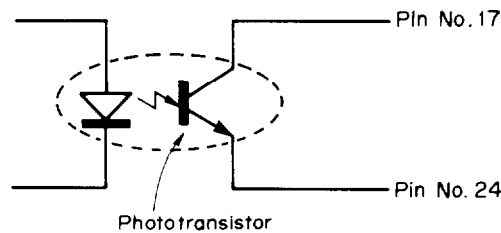
- Notes:** 1. SPACE/MARK signal polarity can be inverted by the DIP switch.
2. High/Low impedance polarity can be inverted by the DIP switch.

(6) With X-ON/X-OFF control

Table 3.7

Data X'fer	RS 232C	Current Loop
Enabled	When X-ON (1 1 H) signal is sent from pin No. 2 of interface connector.	When X-ON (1 1 H) signal is sent across pin No. 17 and pin No. 24 of interface connector.
Disabled	When X-OFF (13H) signal is sent from pin No. 2 of interface connector.	When X-OFF (13H) signal is sent across pin No. 17 and pin No. 24 of interface connector.

- Notes:**
1. The X-ON signal is transmitted repeatedly at time intervals after the power switch is turned on.
 2. LOW and HIGH impedances in current loop are as illustrated below.



LOW impedance: Photo transistor turns ON
 HIGH impedance: Photo transistor turns OFF

Fig. 3.5 Photo coupler

3. About the voltage across pin No. 17 and pin No. 24 in Current Loop Interface
 Since the with stand voltage of the photo transistor shown above is 27V, be careful not to apply a voltage of move than 27V to pin No. 17 and pin No. 24.

3.2.2.2 Condition setting on the interface board

(1) DIP switches setting

The RS-232C/Current loop interface board is equipped with four DIP switches. The specifications of DIP 1 and DIP 2 are the same as those on the other interface boards.

A. DIP 1 : Refer to 3.1.2.2

B. DIP 2 : Refer to 3.1.2.2

C. DIP 3 : Refer to the following table

Table 3.8 Setting of DIP 3

DIP 3	Function	ON	OFF	Factory Setting
3-1	Not used		Always OFF	OFF
3-2	Buffer operation	Enabled	Disabled	ON
3-3	Buffer recovery timing 1	Table 3.9		OFF
3-4	Buffer recovery timing 2			OFF
3-5	Self-Test operation	Enabled	Disabled	OFF
3-6	Self-Test selection	Line monitor	Loop back	OFF

Buffer recovery timing (DIP 3-3/4)

Table 3.9 Buffer recovery timing

Vacant area for bytes in the buffer	DIP 3-3	
152	OFF	OFF
288	OFF	ON
560	ON	OFF
1936	ON	ON

D. DIP 4 :

Table 3.10 Setting of DIP 4

DIP 3	Function	ON	OFF	Factory Setting
4-1	Word length selection	7 bits	8 bits	OFF
4-2	Parity check	Enabled	Disabled	OFF
4-3	EVEN/ODD Parity selection	Even	Odd	OFF
4-4	Flag polarity selection	Negative	Positive	OFF
4-5	Bit rate selection	Table 3.11		OFF
4-6				OFF
4-7				OFF
4-8				OFF

Bit rate selection (DIP 4-5/6, 5/7, 5/8)

Table 3.11 Bit rate selection

Bit rate (BPS)	DIP SW pin			
	SW4-5	SW4-6	SW4-7	SW4-8
75	ON	ON	ON	ON
110	ON	ON	ON	OFF
134.5	ON	ON	OFF	ON
150	ON	ON	OFF	OFF
200	ON	OFF	ON	ON
300	ON	OFF	ON	OFF
600	ON	OFF	OFF	ON
1,200	ON	OFF	OFF	OFF
1,800	OFF	ON	ON	ON
2,400	OFF	ON	ON	OFF
2,400	OFF	ON	OFF	ON
9,800	OFF	ON	OFF	OFF
19,200	OFF	OFF	ON	ON

(1) Jumper wire connection

Table 3.12 Jumper wire connection

Jumper	Description	At delivery
J1	Connects CTS (transmission enable) to +12V. (Note 1)	ON
J2	Connects DSR (data set ready) to +12V. (Note 2)	ON
J3	Connects DCD (carrier detect) to +12V. (Note 3)	ON
J4	Connects TTY RXD to +12V via 470Ω. (Note 4)	ON
J5	Connects TTY RXD RETURN to GND. (Note 4)	ON
J6	Connects TTY TXD RETURN to GND. (Note 5)	ON
J7	Connects TTY TXD to +12V via 470Ω. (Note 5)	ON
J8	Set to ON when μPD7810 is used as CPU. (Note 6)	ON
J9	Set to ON when μPD7811 is used as CPU. (Note 6)	OFF
J10	Transmits X-ON/X-OFF. (Note 7)	ON
J11	Does not transmit X-ON/X-OFF. (Note 7)	OFF
J12	2 K-byte RAM is used. (Connected at the factory.) (Note 8)	ON
J13	8 K-byte RAM is used. (Note 8)	OFF
JX	X-ON/X-OFF is used in current loop. (Note 9)	ON
JF	Flag control is used in current loop. (Note 9)	OFF
JRS	RS-232 is used. (Note 10)	ON
JCL	Current loop is used.	OFF

Note 1: TXD cannot be output unless CTS is ON (positive voltage)

Notes 2 and 3: RXD cannot be received unless both DSR and DCD are ON (positive voltage)

Note 4: Jumpers 4 and 5 are used when current loop in the host computer is not connected to power supply.

Note 5: It is used when the current loop in the host computer side is not supplied with power. Other than the above case (when RS232C or the current loop in the center machine side is given the power source), disconnect J4 - J7.

Note 6: Either J8 or J9 must be jump-connected (ON) alternatively. Its ON/OFF setting differs according to the CPU at delivery.

Note 7: Either J10 or J 1 1 must be jump-connected (ON) alternatively. With J10 ON, as X-ON/X-OFF is transmitted, when the reception line of the center machine is open, the input buffer may be overflowed.

Note 8: Either J12 or J 13 must be jump-connected (ON) alternatively.

Note 9: Either JX or JF must be jump-connected (ON) alternatively.

Note 10: Either JRS or JCL must be jump-connected (ON) alternatively.

3.2.2.3 Pin assignment of interface connector

A. CN1 : .This connector communicates CN1 of the UXMCL board

Refer to 2.3.1.

B. CN2: Future specification

C. CN3: This connector communicates with the Host Computer.

(1) Number of pins: 25 pin cannon type

Table 3.13 Pin assignment (CN3 of IURS)

Pin No.	Signal Name	Direction	Description
1	Protective Ground	—	Chassis ground
2	Transmitted Data (TXD)	Out	Transmitted serial data
3	Received Data (RXD)	In	Received serial data
6	Data Set Ready (DSR)	In	This signal must be at the positive EIA level for the printer to receive data.
7	Signal Ground	In	Return path for data and control signals.
8	Data Carrier Detect (DCD)	In	This is the same signal as DSR at pin No. 6. DCD and DSR can be held at SPACE internally. The signal polarity is factory set to SPACE.
11	Reverse Channel (= 2nd RTS)	Out	This signal is at the positive EIA level when the printer is ready to accept data entry, and at the negative EIA level when the printer is not ready to accept data entry. Operator can invert the polarity of this signal by the DIP switch pin No. 1-4.
20	Data Terminal Ready (DTR)	Out	
17	TTY-TXD	OUT	Low impedance (MARK) between pin Nos. 17 and 24 or X-ON signal sent across pin Nos. 17 and 24 indicates that the printer is ready to accept data; High impedance (SPACE) or X-OFF signal being sent indicates that the printer is busy. Operator can invert the polarity of this by the DIP switch pin No. 1-4.
24	TTY-TXD Return		
25	TTY-RXD	In	Input data of serial current loop.
23	TTY-RXD Return	—	

Notes:

1. "Direction" refers to the direction of signal flow as viewed from the printer,
2. All signals except TTY-TXD and TTY-RXD are based on EIA RS-232C level.

3.2.3 Operating principle

3.2.3.1 Data entry

Serial data entry is performed under the preset conditions.

- (1) The serial data transferred from the host computer is input to CN3 pin 3 (RXD) or pin 25 (TTY RXD).
- (2) The data input to pin 3 (RXD) or pin 25 (TTY RXD) is entered in the CPU. Then, the data is converted from serial to parallel inside the CPU.
- (3) The converted parallel data is stored in the 2 K-byte input buffer.
Concerning this stored data, its status is made known to the host computer (flag control or X-ON/X-OFF control) after performing buffer full/empty control.
- (4) The stored data is transferred to the print buffer via 8255AC-5 (peripheral interface) as required.

3.2.3.2 Buffer full/empty control

(1) Flag control

The status flag is used for handshaking with the host computer. (When a status flag is emitted, data entry to the 2 K-byte buffer is possible.)

a) Using RS232C

When the rest of the 2 K-byte input buffer become 16 bytes, interface connector CN3 pin 11 (REV) and pin 20 (DTR) go mark state, telling the host computer that the buffer is full.

Data is processed after it has been. When the set value of the buffer recovery timing corresponds with the bytes available in the buffer, pins 11 and 20 go LOW, signaling the host computer that data entry is possible.

b) Using current loop

The operating principle is the same as for RS-232C. However, when the 2 K-byte buffer is full, the impedance between interface connector CN3 pins 17 (TTY TXD) and 24 (TTY TXD R) is made HIGH to tell the host computer that the buffer is full. When the set value of the buffer recovery timing (DIP 3,3-4) corresponds with space available in the buffer, impedance between pins 17 and 24 is made LOW, telling the host computer that data entry is possible.

(2) X-ON/X-OFF control

In the X-ON/X-OFF control, when data entry is possible, DC1 (X-ON) is transmitted to the host computer, while when impossible, DC3 (X-OFF) is transmitted.

a) Using RS-232C

X-ON (DC1 : 11 H) is periodically (every 8 bytes) transmitted from interface connector CN3 pin 2 (TXD) until the remaining space for the serial data stored in the 2 K-byte buffer via RXD is for 16 bytes. Thus, the host computer is informed that data entry is possible.

When the remaining space for the data is 16 bytes, X-OFF (DC3: 13H) is transmitted from TXD. Thus, the host computer is informed that the buffer is full.

b) Using current loop

X-ON is transmitted from interface connector pins 17 (TTY TXD) and 24 (TTY TXD R) every 8 bytes until the rest space for the serial data stored in the 2 K-byte buffer through TTY RXD and TTY RXD R is for 16 bytes. When it is for 16 bytes, X-OFF (DC3: 13H) is transmitted from TTY TXD and TTY TXD R.

(3) Flag set/reset, X-ON/X-OFF sequence

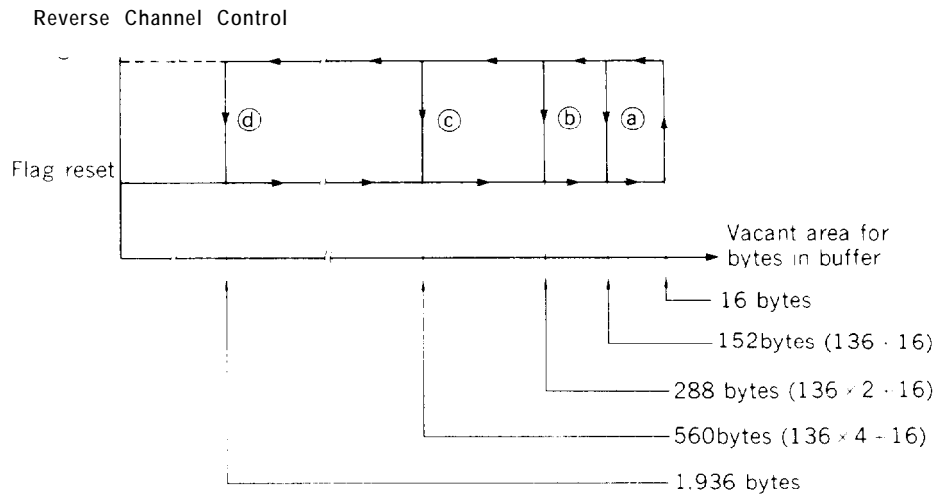


Fig. 3.6 Flag set and reset timings

a) As shown in Fig. 3.6, the flag timing is set when 16 bytes remain in the buffer. At the same time, X-OFF is transmitted and the subsequent data input is prevented. However, even when the rest of buffer is for 16 bytes, data entry is possible until the buffer is completely full (total capacity, 2 K-bytes).

b) When the print processing begins after data entry is prevented, the space in the buffer increases gradually.

As space remaining in the buffer increases, the flag is reset and X-ON is transmitted at the preselected point timing (a, b, c or d, Fig. 3.6).

- Timing (a): buffer rest space for 152 bytes
- Timing (b): buffer rest space for 288 bytes
- Timing (c): buffer rest space for 560 bytes
- Timing (d): buffer rest space for 1936 bytes

Even after the flag is set or X-OFF is transmitted, data entry is possible until the rest of buffer becomes 16 bytes. However, after this, subsequent data are cut off.

(4) Bit rates and X-ON/X-OFF transmit timing

Table 3.14
Bit rates and X-ON/X-OFF transmit timings

Bit rate	X-ON/X-OFF
75	1.06 sec.
110	0.72 sec.
134.5	0.59 sec.
150	0.53 sec.
200	0.40 sec.
300	0.26 sec.
600	0.13 sec.
1,200	66.0 msec.
1,800	44.0 msec.
2,400	33.0 msec.
4,800	16.5 msec.
9,600	8.3 msec.
19,200	4.1 msec.

At the above timing, X-ON/X-OFF is transmitted with an interval 80 times the width of one bit cell, i.e. for the data of 10 bits/character, X-ON/X-OFF is transmitted every 8 characters. In addition, when the state of X-ON/X-OFF shifts, the timing is as follows:

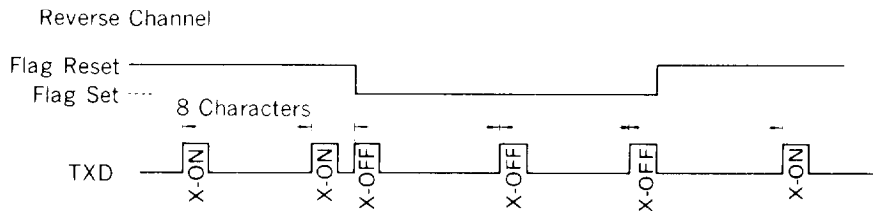


Fig. 3.7 TXD timing in X-OFF/X-ON transition

3.2.3.3 Self-test

The printer self-test can be performed in either of two modes: Loopback or line monitor. The self-test mode be selected by setting DIP switch pins 2-5 and 2-6 on the interface board. Refer to Table 3.15, for setting specifications.

Table 3.13 Loopback/Line monitor

SW2-5	SW2-6	Mode
ON	OFF	Loopback
ON	ON	Line monitor

(1) Loopback Mode:

To enter the Loopback Mode, refer to Table 3.13, and set the DIP switches: then, turn the power on.

When the power is switched on, interface connector pins 2 and 3, TXD and RXD, respectively, are connected, and data from 20H to 7EH are transferred from pin 2 to pin 3 and are printed by the printer. (This sequence of events is only operational when the RS 232C data input level has been selected. It does not occur in the current loop mode.)

(2) Line Monitor Mode

In Line Monitor mode, data on the RS-232C line are printed in hexadecimal code. The timing of Buffer Full Recovery is determined by the DIP switch setting. The only difference from the normal processing is that data is printed after it is converted to hexadecimals

3.2.3.4 Miscellaneous function

(1) Printer error

a) Parity error

Turning DIP 4-2 (ON/OFF) implements the parity check. The check is performed at the CPU for serial data input. When a parity error is detected, an asterisk "*" is printed in lieu of the selected character.

b) Status error

When the printer runs out of paper, the flag is set or X-OFF is transmitted immediately informing the host computer that data transfer has been disabled.

c) Flaming error

A flaming error is caused when the stop bit is not recognized by the printer because of the incorrect handshake setting between host computer and printer. If the flaming error occurs, the data from host computer will be ignored and incorrect printing will occur.

3.2.4 Block diagram

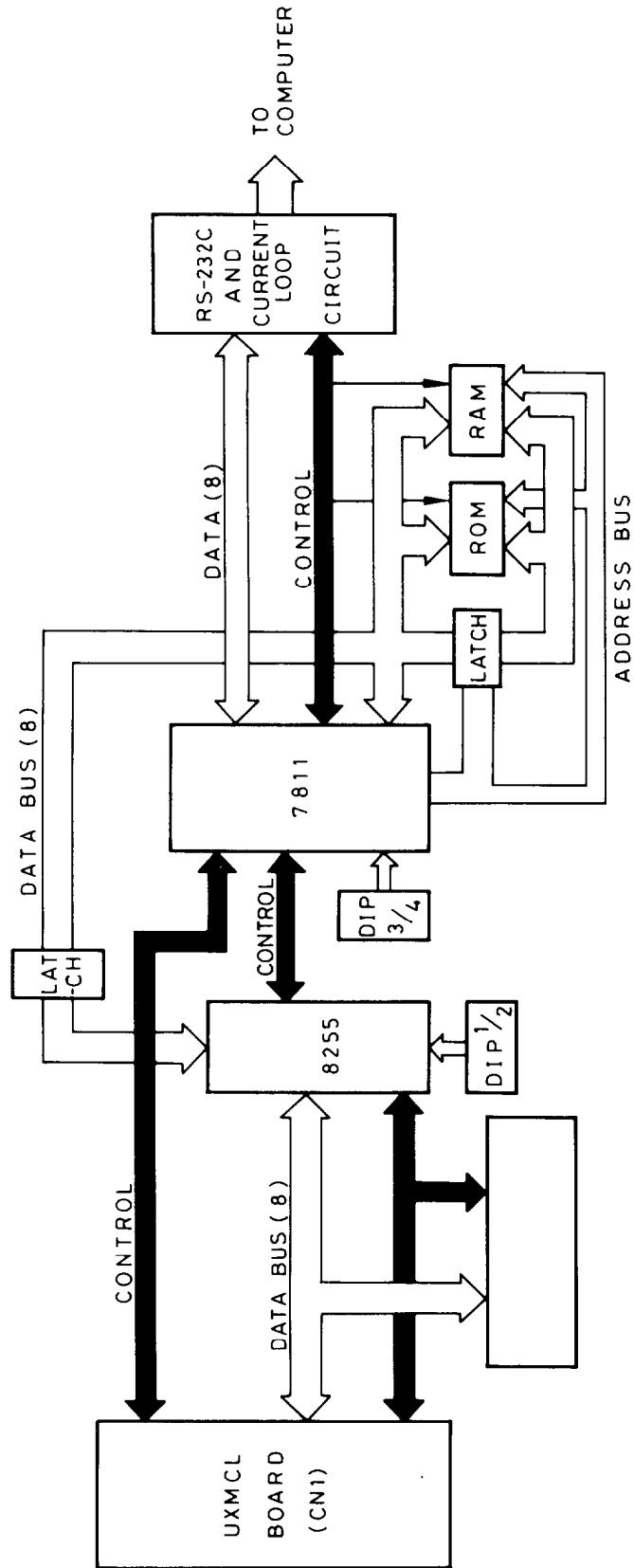


Fig. 3.8 IURS block diagram

3.2.5 Circuit diagram

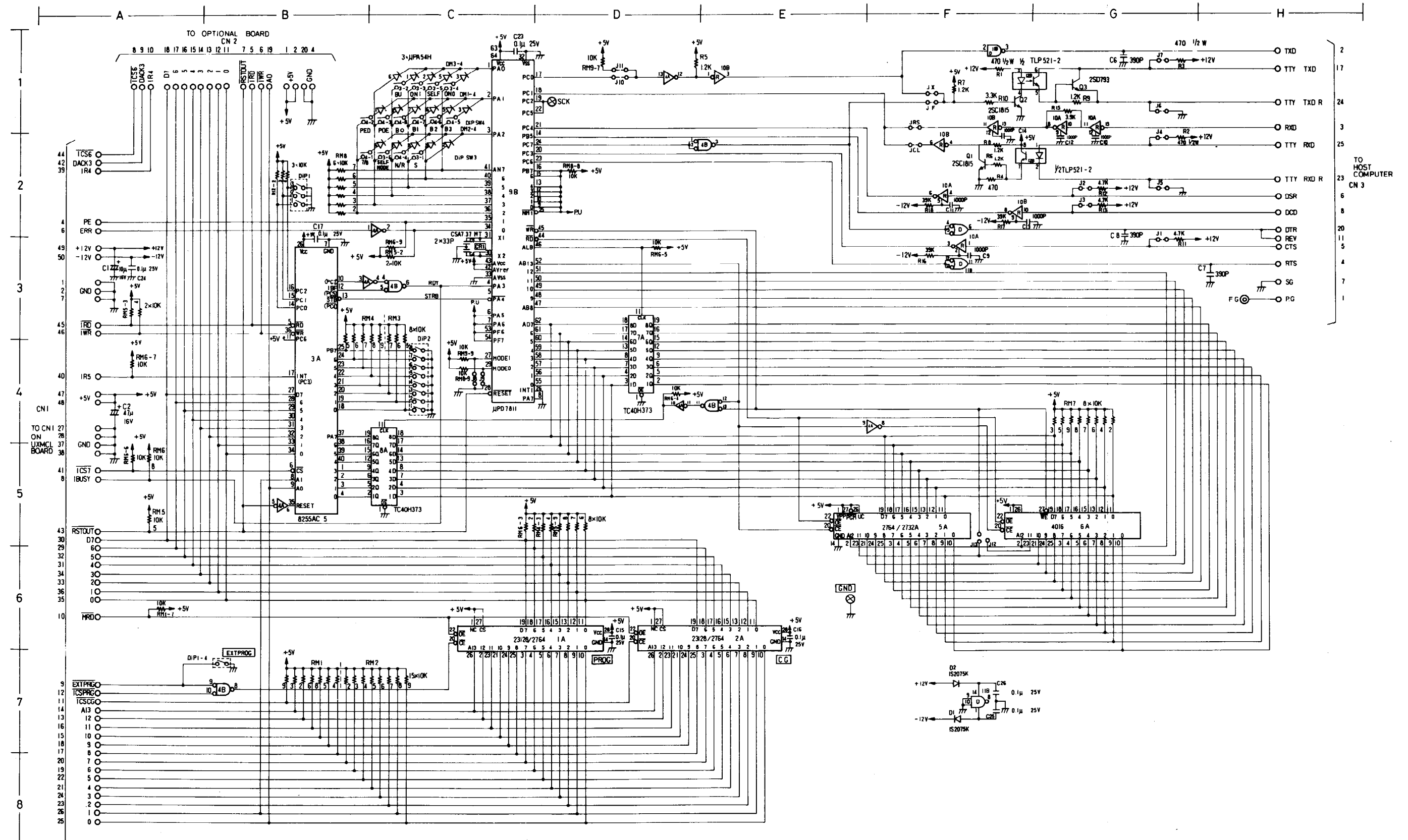


Fig. 3.9 IURS circuit board

IURS CIRCUIT BOARD
UNIT NO. Y4952030000

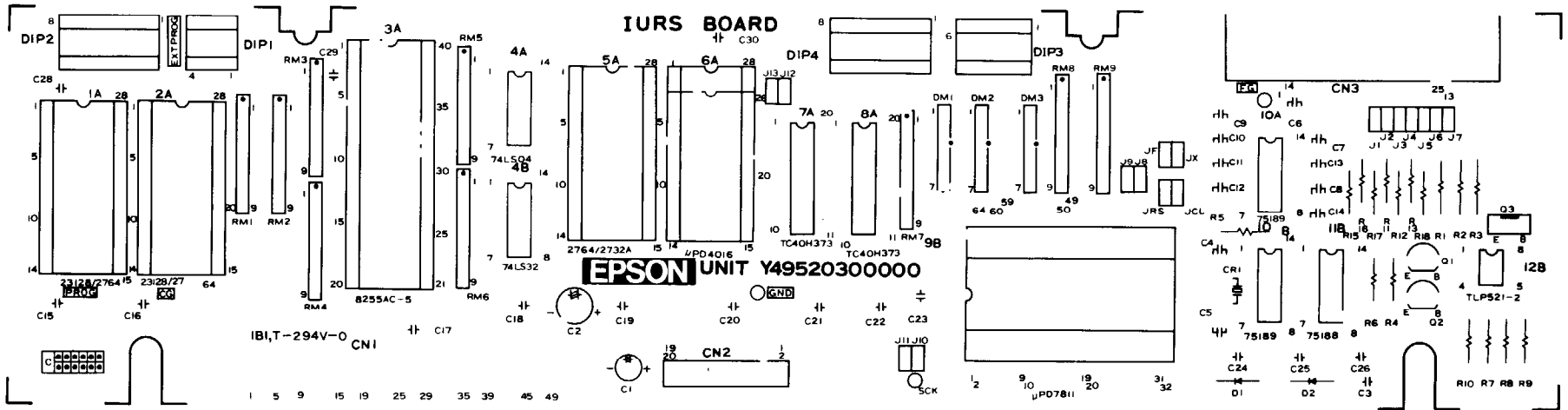


Fig. 3.10 Component layout of IURS board

3.3 IEEE-488 Interface (Cat. No. 7165)

3.3.1 Introduction

IEEE-488 Interface Unit incorporates a CPU and has a 2K-buffering function. This interface allows an IEEE-488 Computer or measuring instrument to produce printed output on an EPSON LQ-1500 dot matrix printer.

3.3.2 Specifications

3.3.2.1 Specification

- (1) Total cable length : 20m Max.
- (2) Cable length between equipment : 5m Max.
- (3) Number of devices that can be connected : 15 Units Max.
- (4) Data exchange method : 3 wire handshaking
- (5) Data, transfer : 8 bit parallel
- (6) Logic convention of signals
True : L level 0.8V Max.
False: H level 2.0V Max.

(7) Interfacing functions provided:

The Intelligent IEEE-488 2K-buffer Interface Board is provided with the following three operations.

a) AH1

The AH1 allows the printer to receive messages on the DIO lines. AH1 includes all the functions of AH. (The subset of the other required functions is L1.)

b) L1

The L1 provides a device with a function to receive data from another device via the interface. This is available only when the device is addressed as a listener.

L1 allows the device to operate when addressed as a listener or in listen-only mode. (The subset of the other required is AH 1.)

c) DC1

The DC1 clears (i.e. initializes) all the devices or the devices or the device addressed as a listener.

DC 1 includes all of DC. (The subset of the other required function is L1 .)

3.3.2.2 Condition setting on the interface board

The IEEE-488 interface board is provided with four DIP switches and four jumpers. Their respective functional settings are as follows:

Setting of DIP Switches

- A. DIP1 See 3.1.2.2
- B. DIP2 See 3.1.2.2
- C. DIP3

Address calculation formula:

$$\text{Address} = 2^4 \times A_5 + 2^3 \times A_4 + 2^2 \times A_3 + 2 \times A_2 + A_1$$

Table 3.16 Setting of DIP SW3

SW Pin No.	Function	ON	OFF	Factory-set condition
3-1	Listen only/address operation selection	Listen only operation	Address operation	OFF
3-2	A5	1	0	OFF
3-3	A4	1	0	OFF
3-4	A3	1	0	OFF
3-5	A2	1	0	OFF
3-6	A1	1	0	OFF

Example: The following example shows how to set printer address "6".

$$6 = 2^4 \times 0 + 2^3 \times 0 + 2^2 \times 1 + 2 \times 1 + 0$$

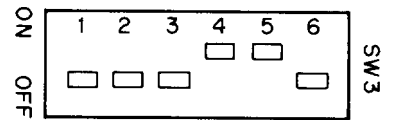


Fig. 3.11 Setting example

- D. DIP4

Table 3.17 Setting of DIP 4

SW Pin No.	Function	ON	OFF	Factory-set condition
4-1	IF board enable	Enable	Disable	ON
4-2	Buffer operation enable	Enable	Disable	ON
4-3	Buffer-full recovery timing	See Table 3.18		OFF
4-4				OFF
4-5	Selection of operation to IFC	IFC + device clear	IFC only	OFF
4-6	Selection of handshaking termination method	Terminates with NRFD = LOW	Terminates with NRFD and NDAC = High	OFF
4-7	Self-test enable	Enable	Disable	OFF
4-8	Selection of self-test method	Bus monitor	Self print	OFF

Setting of buffer-full recovery timing

Buffer-full recovery timing is controlled by setting DIP switch 4, pins 3 and 4 (Table 3.18). Once the buffer is full, data entry will not be resumed until the buffer can again accommodate the number of bytes designated by the switch setting.

Table 3.18
Setting of DIP SW Pins 4-3 and 4-4

Number of bytes	DIP SW Pin No.	
	4-3	4-4
152	OFF	OFF
288	OFF	ON
560	ON	OFF
1,936	ON	ON

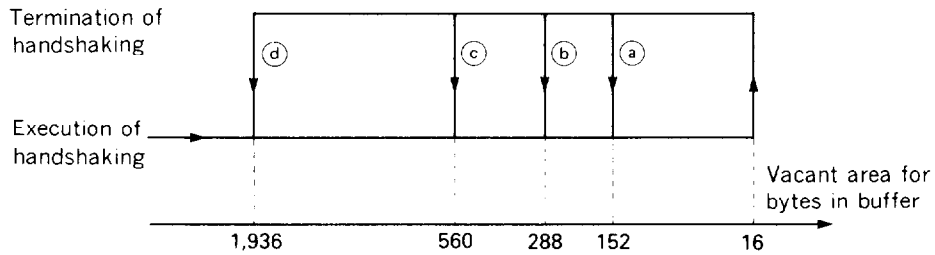


Fig. 3.12 Buffer operation

3.3.2.3 Pin assignment of interface connector

- A. CN 1 : Connected to UXMCL circuit board
- B. CN2: Future specification
- C. CN3: Connected to Host Computer

Table 3.19 Pin assignment (CN3 of IUIE)

Pin No.	Signal Name	Description
1	D101	Data bit 1 of 8-bit parallel data bus
2	D102	Data bit 2 of 8-bit parallel data bus
3	D103	Data bit 3 of 8-bit parallel data bus
4	D104	Data bit 4 of 8-bit parallel data bus
5	EOI	End or Identify (Not used)
6	DAV	Data Valid (Signal from Talker or Controller)
7	NRFD	Not Ready for Data (High = interface waiting for data)
8	NDAC	Not Data Accepted. (High completion of data acceptance.)
9	IFC	Interface Clear
10	SRQ	Service Request (Not used)
11	ATN	Attention (Data/Command Mode Select) (Low command mode)
12	SHIELD	Shield of interface cable
13	D105	Data bit 5 of 8-bit parallel data bus
14	D106	Data bit 6 of 8-bit parallel data bus
15	D107	Data bit 7 of 8-bit parallel data bus
16	D108	Data bit 8 of 8-bit parallel data bus
17	REN	Remote Enabl
18	GND6	Ground
19	GND7	Ground
20	GND8	Ground
21	GND9	Ground
22	GND10	Ground
23	GND11	Ground
24	LOGIC GND	Ground for logic

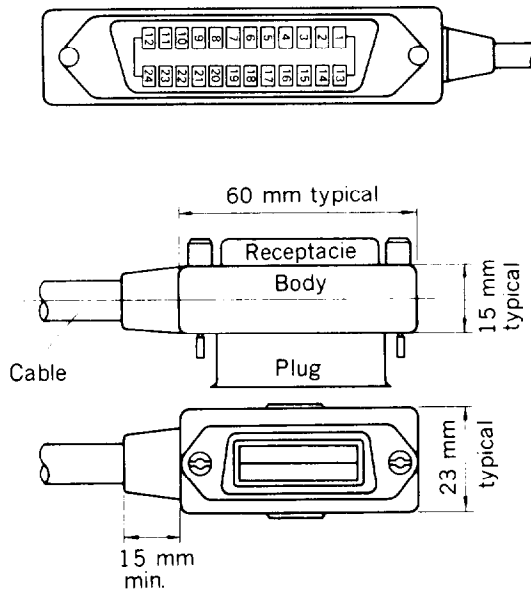


Fig. 3.13 IEEE-488 connector

3.3.3 IEEE-488 operational parameters

3.3.3.1 Handshaking

Setting DIP switch pin No. 3-1 adjusts parameters for handshaking to either address (3-1 OFF) or listen only (3-1 ON) mode.

(1) Address Operation Mode

With DIP switch 3-1 OFF, data entry is enabled when a LOW attention (ATN) signal is emitted from the controller, and the printer is designated as listener.

With this switch setting (3-1 OFF), data entry may be disabled only when:

1) The listen only mode has been designated.

The printer is released from the listen only mode of operation by either a UNL or Interface Clear (IFC) signal. However, the signal messages are not effected until the printing operation in process is completed, using up whatever print data still remains in the buffer.

2) Handshaking is stopped due to a buffer full signal.

When DIP switch pin 4-2 is OFF, handshaking can be stopped by a LOW Not Ready for Data (NFRD) signal while the printer is busy. (Note: Pin 4-2 disables the buffer.)

3) DIP switch 4-2 is ON and the buffer has reached its maximum data capacity.

(See Section 2. Buffer Operation.)

4) The printer is off-line or out of paper.

Data entry is disabled during periods when the printer is off-line or when the paper supply is depleted, by using one of two switch setting options: Setting DIP switch pin 4-6 to ON terminates handshaking when the NFRD signal goes LOW; NFRD and Not Data Accepted (NDAC) go HIGH.

(2) Listen Only Mode

In this mode, the printer receives data whether it has been designated by the controller as a listener or not. Data entry is disabled using DIP switches 4-2 and 4-6 as described in sections 2, 3, and 4 above.

3.3.3.2 Buffer Full/Empty operation

Buffer-full recovery timing is controlled by setting DIP switch 4, pins 3 and 4 (Table 3.18). When maximum buffer capacity remaining is 16 bytes, NFRD goes LOW and handshaking and data entry is terminated. Data entry will not be resumed until the buffer can again accommodate the number of bytes designated by the switch setting (Fig. 3.12. Buffer Operation) and IFC or ATN goes LOW, re-initiating handshaking.

3.3.3.3 Self-test

The printer self-test can be performed in one of two modes (1) Self-Print and (2) Bus Monitor. This self-test mode is selected prior to power up by setting DIP switch pins 4-7 and 4-8 on the IUIE interface board. The switches are read at initialization.

(1) Self-Print Mode

(Switch Settings: 4-7 ON: 4-8 OFF)

Print data 20H to 7EH are continuously printed in hexadecimal code until the power switch is turned Off.

(2) Bus Monitor Mode

(Switch Settings: 4-7 ON: 4-8 ON)

All data on the D10 lines of the IEEE-488 bus are transferred to the printer as parallel 8-bit words for printing in hexadecimal code. If it is command data, ATN HIGH, the information is printed out in emphasized/underlined print mode; if it is data, ATN LOW, information is printed in normal mode.

Print sample

3F 55 2A 41 42 43 OD OA

Command Data

3.3.4 IEEE-488 functional commands

(1) Only two of the IEEE-488 commands are utilized with the IUIE interface board: Selected Device Clear (SDC), which resets the printer; and Device Clear (DCL), which clears the print data stored in the buffer. All other commands generally associated with the standard are ignored by the interface board.

Operation of Interface to IFC

The Interface Clear (IFC) signal operation mode parameters are set via DIP switch 4, pin5. When IFC is input with switch 4-5 ON, both the interface board and printer are cleared; When the switch is OFF, only the interface board is cleared.

(2) Remote/Local Operation

The ON- and OFF-LINE states of the printer are independent of the remote/local designation by the IEEE-488. Therefore, switching of the printer from OFF-LINE to ON-LINE state is not performed via a message from the host computer.

Normally, in local mode, the printer is not required to respond to a remote message. However, if the printer is connected to a controller whose REN signal is LOW, the printer will respond by performing a printout, even though the local mode is in effect.

(3) IEEE-488 handshake sequence

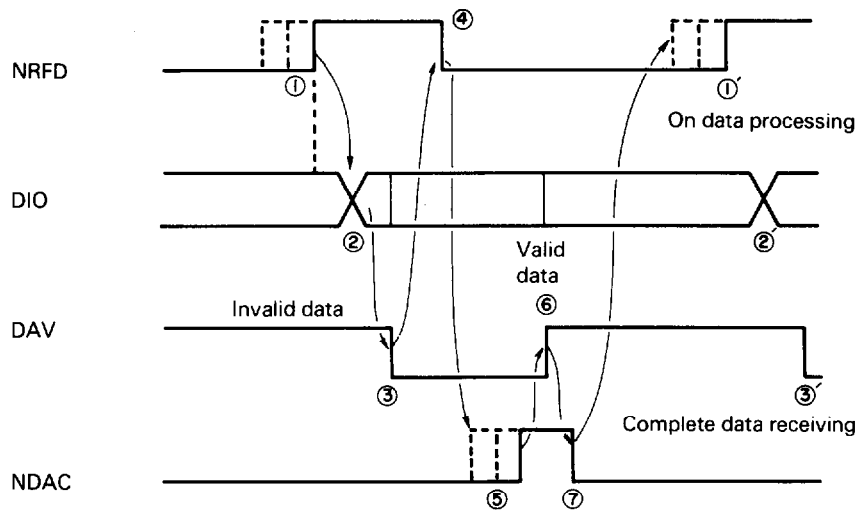


Fig. 3.14 Timing chart of 3 wire handshaking

Description of handshake timing

- 1) Listener waits for data.
- 2) Talker transmits data to data line.
- 3) Talker checks NRFD.
DAV must be LOW NRFD HIGH.
- 4) Listener reads data with DAV LOW.
NRFD is made LOW for data processing.
- 5) NDAC is made HIGH when listener completes data reception.
- 6) Talker makes DAV HIGH to tell listener that data bus is disabled.
- 7) Listener makes NDAC LOW with DAV HIGH to complete handshake in the state that data is not received.

3.3.5 Block diagram

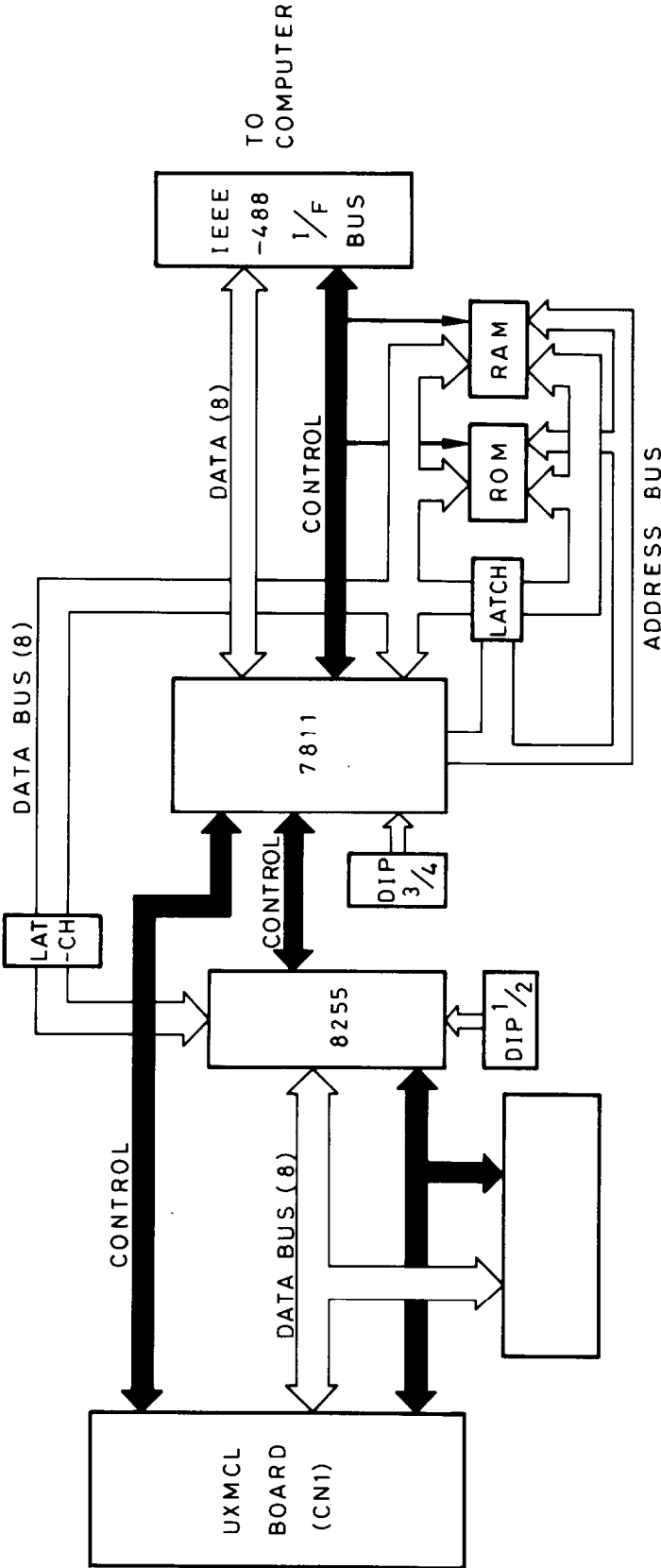


Fig. 3.15 IUIE block diagram

When data is exchanged between the main board (UXMCL) and IUIE boards, the uPD781 1 controls data exchange as the central processor in the IUIE board. The data transferred from the IEEE-488 computer or measuring equipment is entered in pPD7811 and then stored in the 2 K-byte RAM. The stored data is entered in the buffer on the main board (UXMCL).

The program for data exchange control is stored in the 4 K-byte ROM. The statuses of DIP 1,2,3 and 4 are each read into memory in the 8255AC-5 or the uPD781 1 at power ON.

3.3.6 Circuit diagram

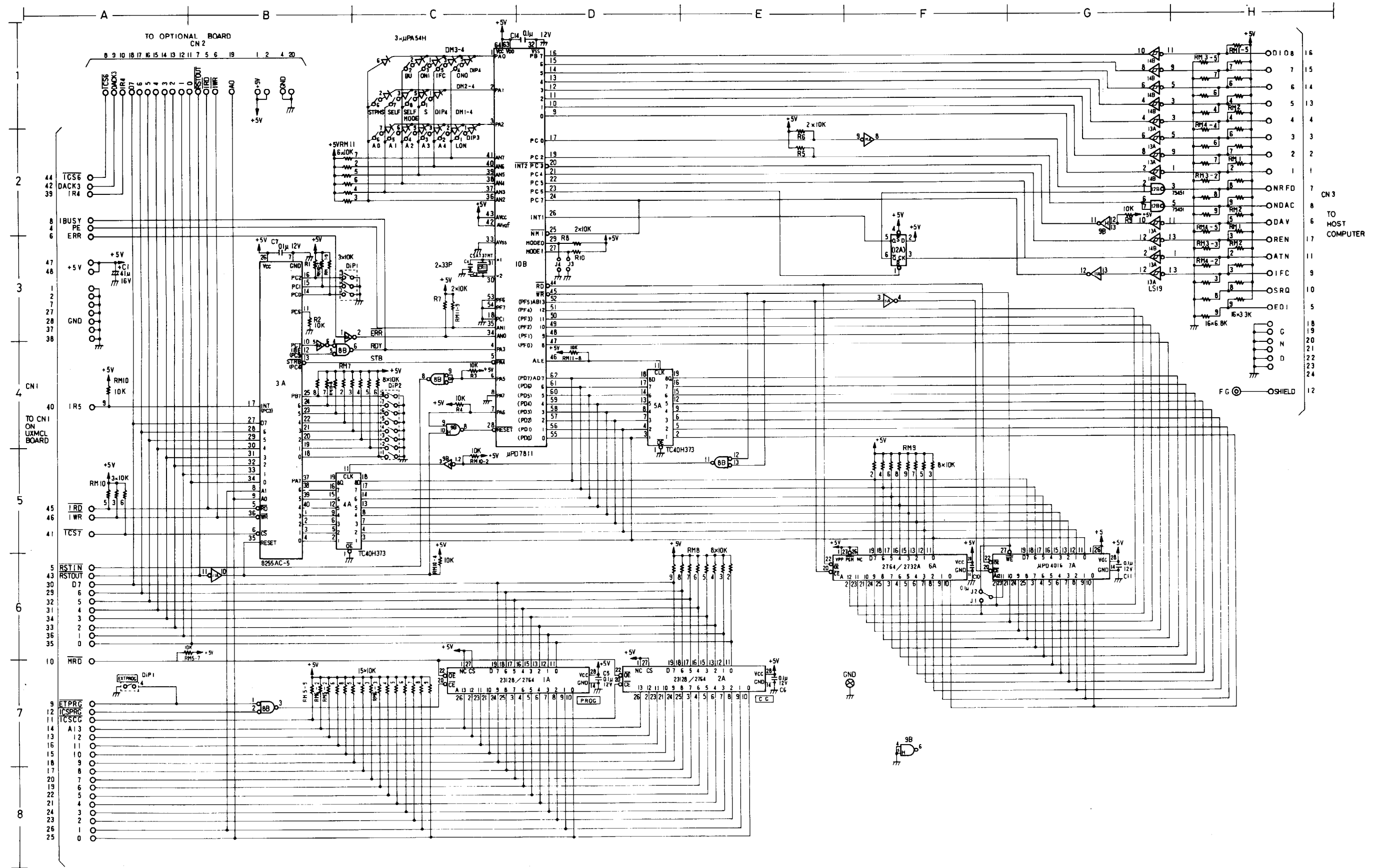


Fig. 3.16 UIE circuit board

UIE CIRCUIT BOARD
UNIT NO.Y4952020000

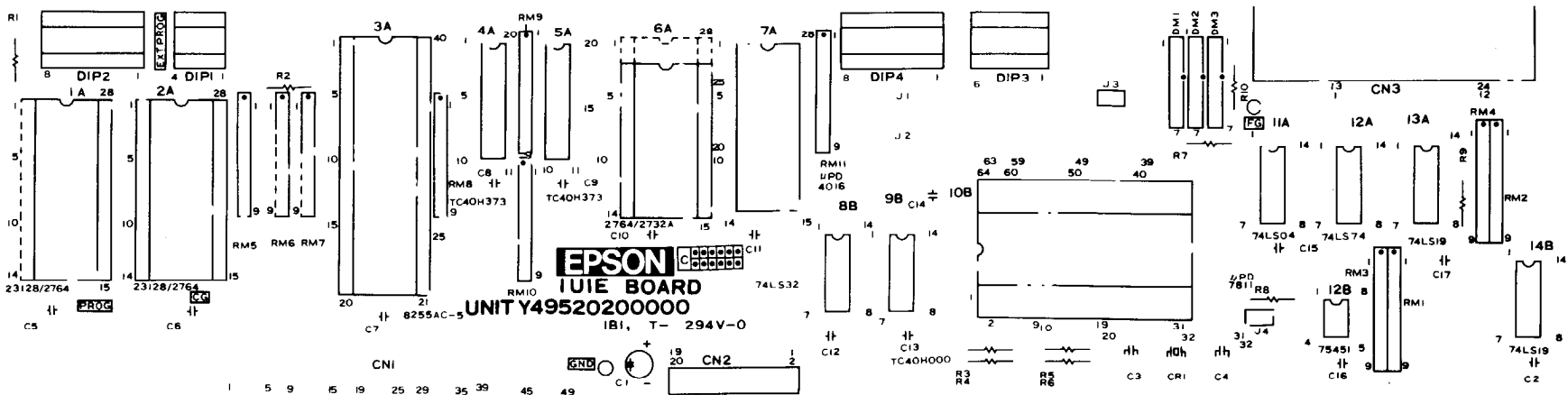


Fig. 3.17 Component layout of IUIE

3.4 Single Bin Cut Sheet Feeder (# 8334) Double Bin Cut Sheet Feeder (# 8344)

3.4.1 Introduction

The EPSON Cut Sheet Feeder #8334, 8344 makes a perfect companion to the LQ-1500 printer. Reliably and automatically feeding paper to the printer one sheet at a time, it greatly enhances the speed and efficiency of letter-quality document preparation.

There are two types of Cut Sheet Feeder: a single bin cut sheet feeder (# 8334), and a double bin cut sheet feeder (#8344). Operating principles, disassembly/assembly and trouble shooting is almost the same. This technical manual deals with double bin cut sheet feeder (# 8344).

3.4.2 Specifications

1. Dimensions and Weight

	Single Bin Cut Sheet Feeder (# 8334)	Double Bin Cut Sheet Feeder (# 8344)
Height	350 mm	350 mm
Depth	306 mm	387 mm
Width	516 mm	516 mm
Weight	3.2 kg	4.4 kg

2. Form length

(1) Minimum:

185 mm (7.25") - bin 1

267 mm (10.5") - bin 2

(2) Maximum:

355 mm (14.0")

3. Form width

180 mm (7.0") min.

368.3 mm (14.5") max.

4. Bin capacity

Up to 220 sheets of 70 kg paper (80 g/m²)

5. Capacity of paper delivery stand

Up to 250 sheets of 70 kg paper (80 g/m²)

6. Environmental condition

(1) Temperature

Operation: 5° to 35°C (Rate of change should not exceed 8°C/hour)

Storage: -30°C to +65°C (Non-condensation)

(2) Humidity

Operation: 20 to 80% (Non-condensation)

Storage: 5 to 85% (Non-condensation)

7. Reliability

(1) MCBF (Mean Cycle Between Failure)

187,500 cycles

(2) MTBF (Mean Time Between Failure)

5,000 hours (with an average usage rate of 300 sheets per 8 hours)

8. Paper specifications

Use paper conforming to the specifications below to assure reliable operation of the cut sheet feeder. Paper which does not conform to the following specifications may be used; however, proper operation is not assured. Test such paper prior to regular use.

Most paper is sensitive to temperature and humidity, and the performance of the paper used with the printer and cut sheet feeder can be adversely affected by these conditions. Store paper properly.

Cut sheet paper

a. Paper weight

52 kg paper (60 g/m²)

86 kg paper (100 g/m²)

b. Tolerance

Paper width tolerance: 0.5 mm (0.020")

Paper must be cut squarely (90°), with a deviation of less than 0°03'.

c. Paper type and quality

Paper used should be plain bond, typewriter quality paper with light wood pulp-content.

Paper should have no wrinkles or other visible defects.

d. Storage conditions

Temperature: 18° to 22°C

Humidity: 40 to 60%

e. Other

Paper with a medium to high pulp content and very light or heavy paper should be operationally tested prior to regular use. Paper with a textured, embossed or glossy surface or "hammered" type paper should also be tested.

3.4.3 Principles of operation

3.4.3.1 General construction

The cut sheet feeder is designed for paper feed from one or two paper feed bins.

The construction of the cut sheet feeder can be broken down in 4 subassemblies:

- Form Guide and Form Transport
- Output Stacker
- Drive Mechanism
- Paper Feed bins

3.4.3.2 General description

Form Guide and Form Transport:

The two side frames are mechanically linked by aluminium extruded profiles, containing the insert chute, the eject chute and the feed bins.

Output Stacker:

One stacker is supplied with the unit and may be attached either to the basket or the second profile, depending on user requirements.

Drive Mechanism:

The cut sheet feeder is a mechanical device which is controlled by printer platen movement.

The complete drive and select mechanism is located on the right hand side frame. Both side frames are protected by detachable, molded plastic covers which cover the mechanical components.

Paper Feed Bin:

The feed bin supports have two locking positions:

- Operating position: In this position the paper in the bin is pressed against the pick-up rollers.
- Load position: This position permits paper installation.

3.4.3.3 Form Guide and Form Transport

Fig. 3-1 8 illustrates the paper guide form and paper transport system. Both paper feed bins are shown in their operating position. (One stacker is supplied with the unit and may be attached to the basket ① or to the second profile ②. (The illustration shows the stacker in both position.))

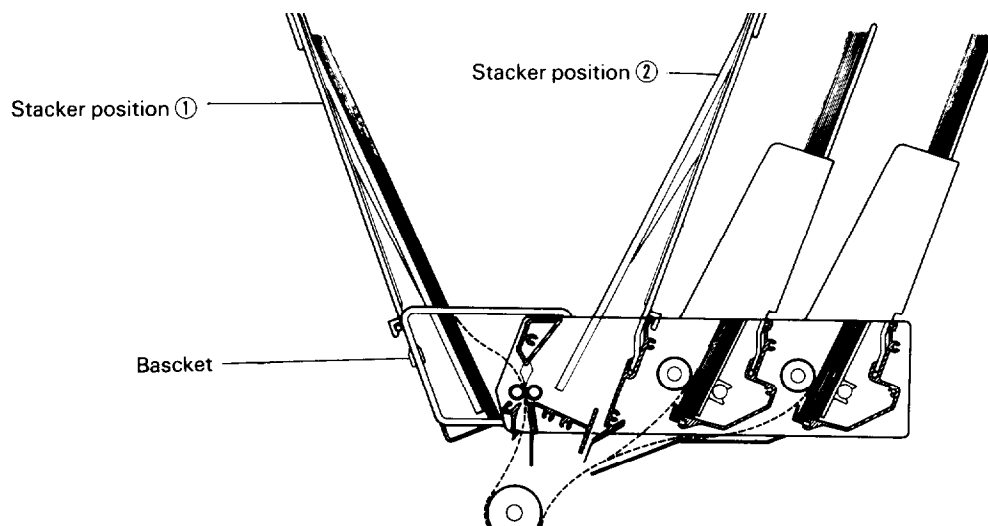


Fig. 3.18 Paper guide and the paper transport system

Both pick-up roller shafts and the eject roller shafts are driven by the printer platen. The platen motion is transmitted through the gear train to the cut sheet feeder.

Two mechanical selection and feed units, one for each pick-up roller shaft, provide the selection of one feed bin and the insertion of a single sheet to the printer platen. Refer also to the operation description of the selection and feed unit.

(1) Insertion from the Feed Bin

After a single sheet is separated by the pick-up rollers, it will be transported through the insert chute to the friction rollers of the printer platen.

(2) Insertion Termination

When the single sheet being transported by the pick-up rollers reaches the platen friction path. The form insertion cycle is terminated.

Once the insertion cycle is completed, paper movement to the first print line and during other print operation will be carried out by printer platen movement only.

During positioning of the form to the first print line, the selection and feed unit will be reset to its home position automatically.

(3) Form Ejection

Printer platen motion will transport the printed form into the eject chute. As soon as the form has reached the eject rollers of the cut sheet feeder it will be transported into the output stacker.

The eject roller shafts are permanently driven by platen motion in forward direction. This keeps the paper tight against the platen.

When the paper is under platen control, the eject rollers slip on the surface of the paper because the friction between the platen pinch rollers and the platen is much stronger than the friction between the cut sheet feeder eject rollers.

As soon as the paper leaves the platen friction path which is about 6 lines from the bottom edge of a page the line spacing will increase by 3%.

(4) Reverse Platen Motion

The printed form will be transported back into the insert chute of the cut sheet feeder if reverse platen motion occurs.

The cut sheet feeder allows a maximum of 1 inch (6 lines) of reverse positioning taking into consideration the following conditions:

1. The positioning of the form to the first print line has been terminated; the selection and feed unit is in its home position.
2. The form is controlled by the printer platen.
3. The number of reverse/forward line spaces is not in that area which permit the selection and feed unit to control paper movement.

(5) Manual Form Insertion

Single sheets, form sets, checks, bank transfers, etc. may be manually inserted, one at a time, using the rear output stacker.

The programmed form insertion cycle must be stopped during manual paper insertion in order to prevent paper jam.

3.4.3.4 Drive mechanism

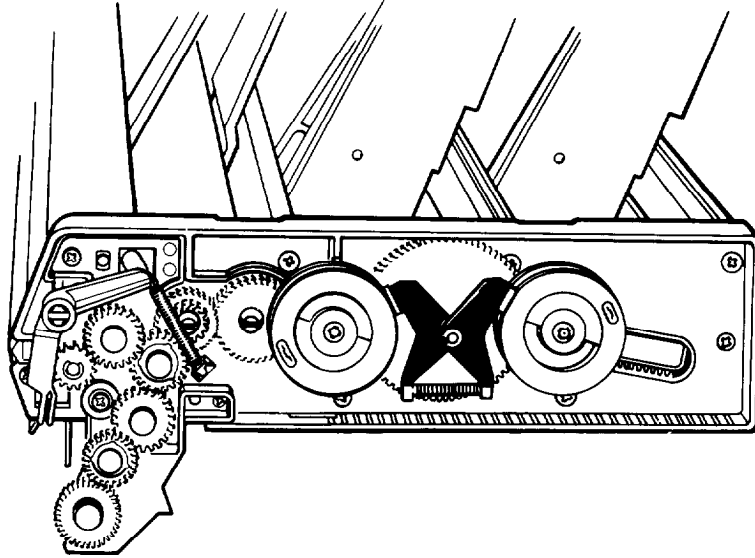


Fig. 3.19 Drive mechanism of the cut sheet feeder

Rotation of the platen shaft gear is transmitted through the idler gears to the eject roller shafts and the selection and feed units of the pick-up roller shafts. Refer to the function description of the selection and feed unit.

Each of these shafts is driven by a one-way clutch which prevents reverse motion of the shafts.

- The eject roller shafts are only driven to transport a form into the output stacker. The pressure of the brake levers prevents uncontrolled motion of the catch plates. The catch plate is a part of the selection and feed unit.

3.4.3.5 Operating the paper bins

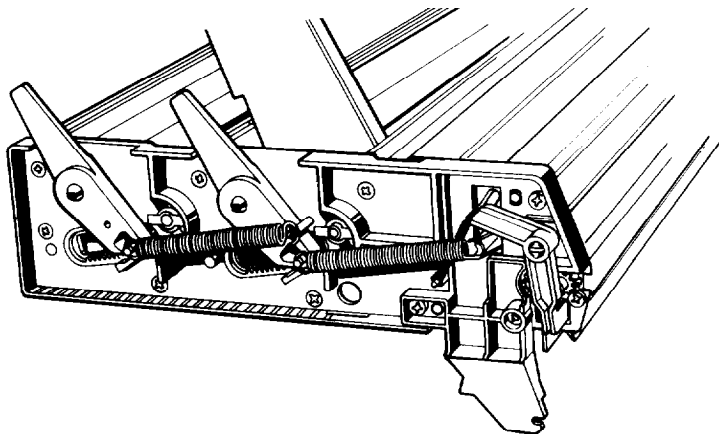


Fig. 3.20 Left side of the feeder

With the left-hand-side release lever the paper bin can be opened for stacking paper. When the bin is closed the feeder will be set to operating condition.

Attention: Each time the paper bin is opened the paper must be stacked again, otherwise the paper will misfeed.

3.4.3.6 Construction and function of the selection and feed unit

The purpose of the selection and feed unit is to select one pick-up roller shaft and transmit the platen motion to this shaft to insert a single sheet until it rests on the platen pinch rollers.

The selection and feed unit is made up of a drive wheel assembly and a catch plate assembly. The drive wheel supports the engaging piece and the selector latch which rotates along the inside cam of the catch plate.

The engaging piece position at the drive wheel defines the home position of the catch plate.

The select mechanism of the catch plate consists of the home position keeper and the turnout spring.

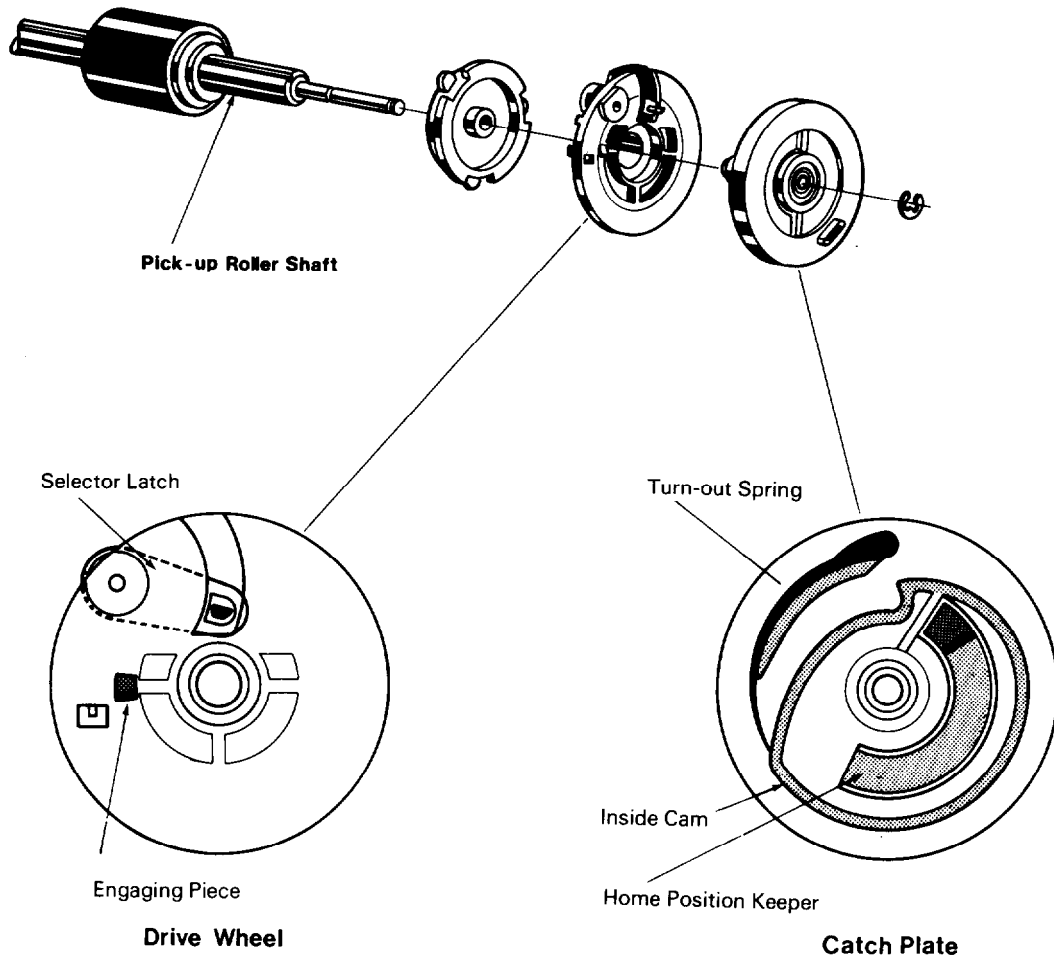


Fig. 3.21 Construction of the selection and feed unit

(1) Operation of the selection and feed unit

The operation of the selection and feed unit can be divided into three main cycles:

- a) Home Position Cycle: Printer platen motion is carried out in forward direction (all drive wheels will always rotate in platen direction). If the home position keeper rests on the engaging piece the catch plate will be rotated synchronously.

Both pick-up roller shafts are held in stop position by the one-way clutches.

b) **Selection Cycle:** Assuming that all selection and feed units are in their home positions the execution of “n” line spaces in reverse direction and two line spaces in forward direction activates one of the selection and feed units. The selector latch of this unit will be engaged with the catch plate.

When “n”= 8 Selection of Bin 1 (Red)*

When “n” = 1 1 Selection of Bin 2 (Blue)

c) **Insertion Cycle:** Assuming that selection and feed unit 2 is activated, platen motion in reverse direction will be transferred by the one-way clutch to the pickup roller shaft 2. Form insertion will be performed from feed bin 2. The selector latch of drive wheel 1 follows the inside cam of the catch plate guided by the turn-out spring.

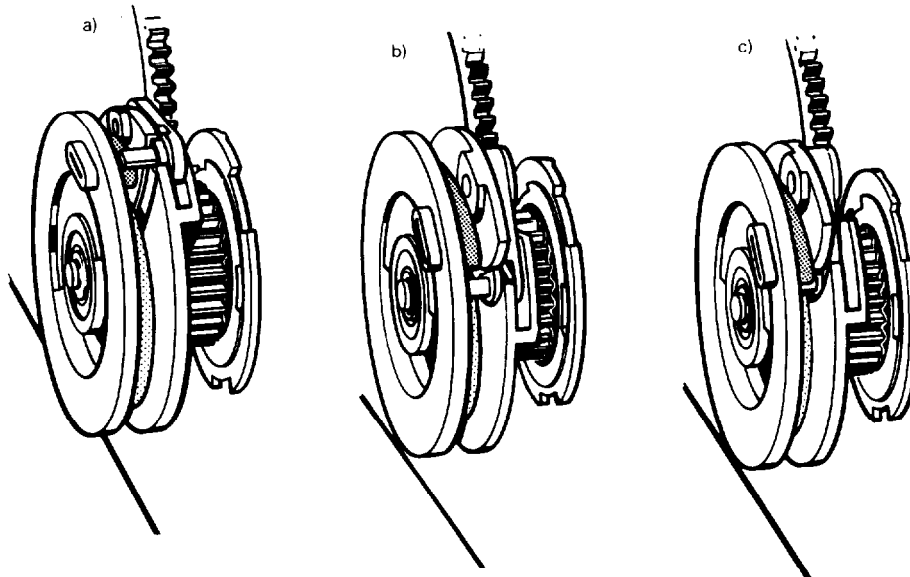


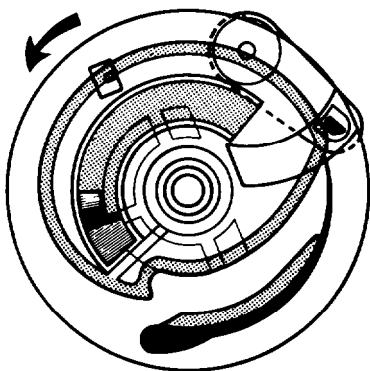
Fig. 3.22 The selector latch follows the inside cam

(2) Detailed description of selection and feed unit operation

In the following schematic diagrams and their associated descriptions, the three main operation cycles are described in detail.

(The term “motion direction” is based on the motion direction of the printer platen.)

a) Home Position Cycle



a The home position keeper rests on the engaging piece of the catch plate. Drive wheel and catch plate will rotate synchronously in a forward direction.

Rotation of the drive wheel in forward direction.

The catch plate will be held stationary by the brake lever until the engaging piece catches the home position keeper.

The catch plate drive is synchronized with the drive wheel movement. The pick-up roller shaft will be held stationary by the one-way clutch.

In order to reach the home position properly, it is necessary to turn the platen forward a maximum of 16 line spaces.

(1 revolution of the drive wheel = 16 line spaces)

Fig. 3.23 Selection and feed unit, home position cycle

* Color designations correspond to the color of the two bin selector mechanisms on the left cut sheet feeder frame.

b) Selection and Insertion Cycle

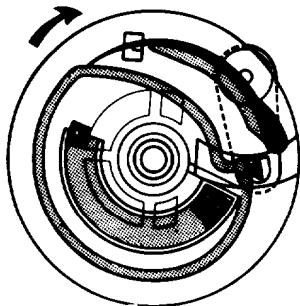


Fig. 3.24 Selection and feed unit selection cycle step 1

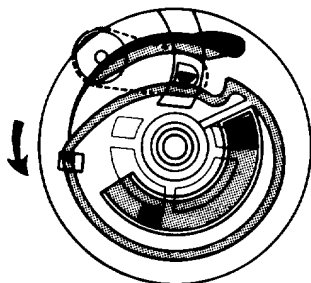


Fig. 3.25 Selection and feed unit selection cycle step 2

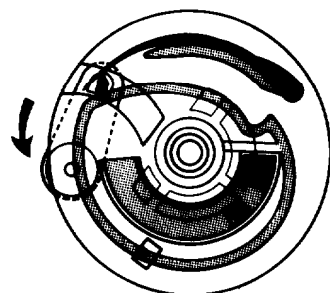
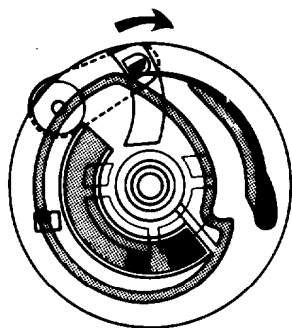
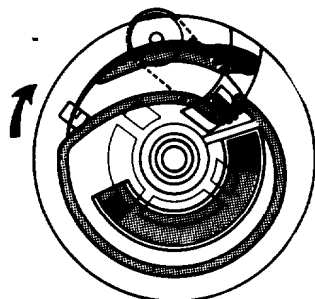


Fig. 3.26 Selection and feed unit, insertion cycle

- One of the selection and feed units is selected.
The corresponding pick-up roller shaft will rotate in reverse direction.
- Platen motion is reversed. After “n” line spaces, the selector latch will drop to the inside cam of the catch plate „

When “n” = 8	Bin 1 (Red one) is selected.
“n” = 11	Bin 2 (Blue one) is selected.

- Change motion direction for a max. of 2 line spaces to position the selector latch on the inside cam below the turn out spring...
- ... Change motion direction again. After approx. 1 line space reverse the selector latch will be engaged with the stop position of the catch plate. The selection and feed unit remains activated until the insertion cycle has been terminated.

The selection and feed unit is activated by applied platen motion to the corresponding pick-up roller shaft.

Carry out of “n” line spaces in reverse direction inserts a single sheet until it rests on the platen with a slight bow in the paper. This bow creates a constant pressure of the sheet being inserted against the platen friction rollers . . .

- | | |
|---------------|-------------------------------|
| When “n” = 34 | Bin 1 (Red one) is selected. |
| “n” = 52 | Bin 2 (Blue one) is selected. |

0 When all drive wheels are driven together, they will be driven synchronously.

The selector latch of the non-activated units will follow the inside cam and pass the turn-out spring.

If the insertion of a single sheet has been terminated the platen should carry out a minimum of 17 line spaces forward, positioning the sheet at the first printable line.

Thereby, the selector latch follows the inside cam pushing the turn-out spring. As soon as the engaging piece catches the keeper, the insertion cycle will be terminated.

Note: The correct termination of an insertion cycle will keep all selection and feed units in their home positions.

3.4.4 Disassembly and assembly

The following tools are required for disassembly and assembly of the cut sheet feeder # 8334/8344.

Tools

Screwdriver (+) # 2

Screwdriver (-) # 2

Pliers for electrical servicing

Precautions

Pay attention to the following points when disassembling and assembling the cut sheet feeder # 8334/8344.

1. Dismount the cut sheet feeder from the printer body before starting disassembly or assembly.
2. Avoid loosening screws other than those specified.
3. For safety, the operator should wear glove.

3.4.4.1 Disassembly

The procedure for disassembling the cut sheet feeder # 8334/8344 is described in this section.

(1) Removal of the basket, stacker, paper stand, side cover, bottom pan, and foot.

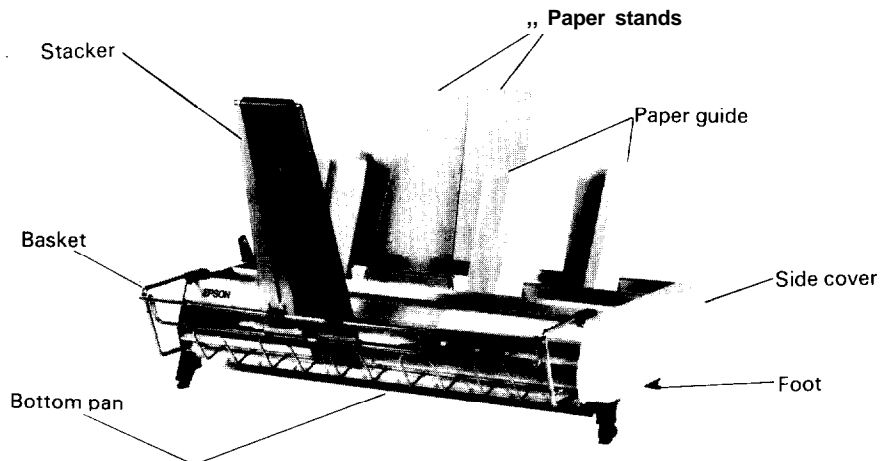


Fig. 3.27

a) Removal of the stacker, paper stands

Hold the base of the stacker, paper stands and lift it up. Bins 1 and 2 and the output stacker can also be removed in the same way.

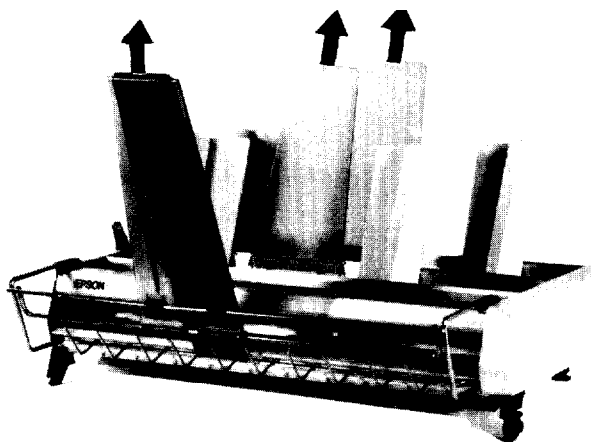


Fig. 3.28 Removal of the stacker

b) Removal of the basket

Hold both ends of the basket and lift up until the basket is removed.

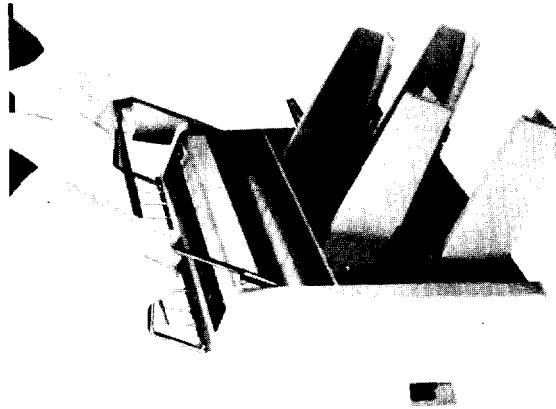


Fig. 3.29 Removal of the basket

c) Removal of the side cover

The side cover is secured to the frame with pawls at three points, two on the top and one on the bottom. Set the release lever free, and open the pawl on the bottom outward. The side cover will then come off. The pawls are positioned at the points shown in the drawing.

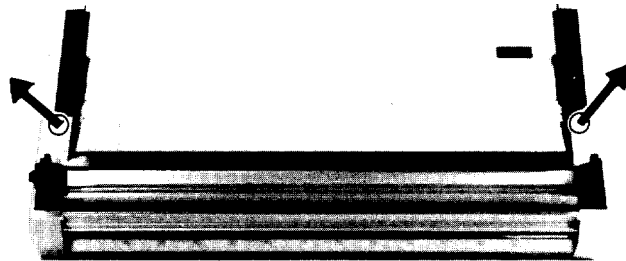


Fig. 3.30 Removal of the side cover (Bottom view of the sheet feeder)

d) Removal of the bottom pan

The bottom pan is simply inserted along the groove from the rear side. It can be removed by pulling outward as shown in the following drawing.

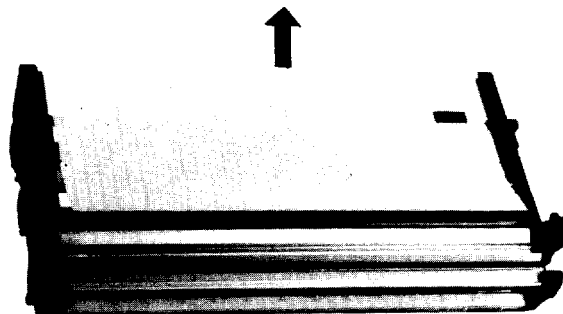


Fig. 3.31 Removal of the bottom pan

e) Removal of the feet

Two feet are used to support the weight of the cut sheet feeder and cut sheets. They are simply inserted into the frame edges from the side. They can easily be removed by pulling them sideways.

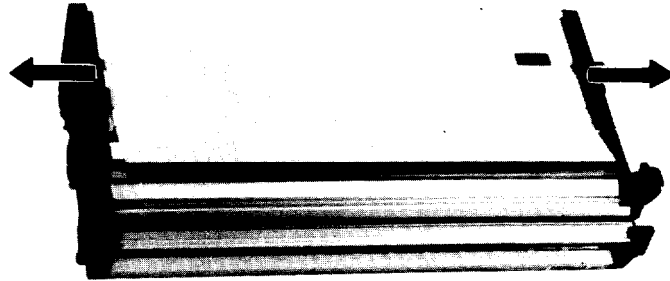


Fig. 3.32 Removal of the feet

(2) Removal of the pressure plates and paper guides

Two paper guides are used in the single bin cut sheet feeder and four in the double bin cut sheet feeder. The paper guide is symmetrical and can be removed in the same way.

Pull the release lever to the side, and secure the pressure shaft.

a) Remove left and right pressure plates.

The pressure plates are mounted so that bin 1 is at the front and bin 2 at the rear; the ribs engage with the pickup roller. Disengage the pressure plate from the pickup roller by moving the plate bottom to the front.

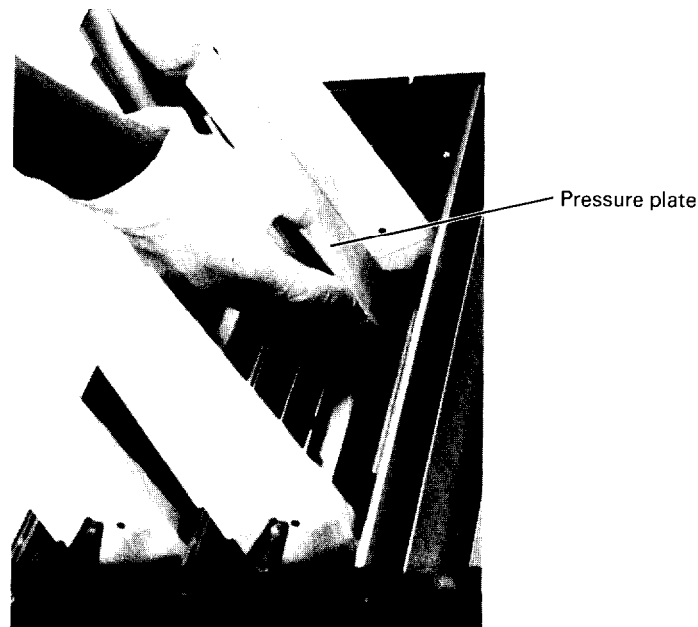


Fig. 3.33 Removal of left and right pressure plates

- b) Remove the clamp on the back of the paper guide.

Insert the screwdriver 9 into the notch on the clamp and force it upward until the clamp comes off. The leaf spring will also be removed.

Note: The clamp is secured very tightly. First pry the clamp with the screwdriver tip to disengage the pawl and then, lift it up with the screwdriver blade.

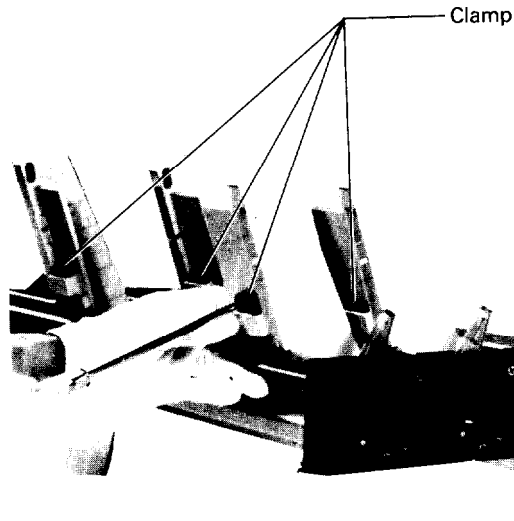


Fig. 3.34 Removal of clamp

- c) Remove Paper Guide @from the Frame.

Remove the paper guide from the frame by moving the paper guide at an angle to the front. Disengage the retaining arm from the frame, push the arm forward, and remove the paper guide.

Caution: If you try to remove the paper guide from the frame with the retaining arm engaged, the retaining arm may break.

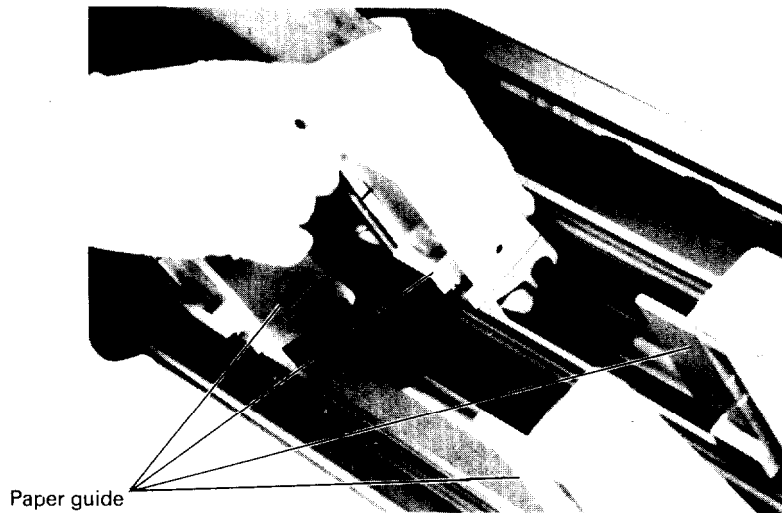


Fig. 3.35 Removal of paper guide

(3) Removing the brake lever, selection/feed unit, gear wheel and pickup roller.

a) Remove the spring attached to the left side of the cut sheet feeder.

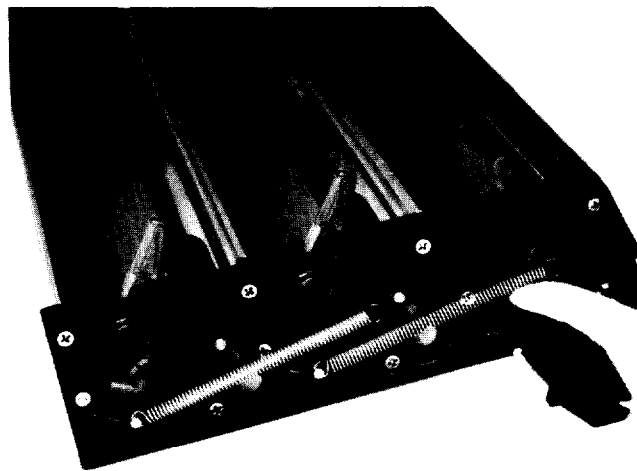


Fig. 3.36 Removal of spring

b) Removal of brake lever attached to the right side.

Remove the spring located between the right and left brake levers. The levers are held on a ribbed peg with a head wider than the circumference of the hole in the brake lever.

Use a pair of pliers to pinch the peg inward so that the levers can be slipped over it.

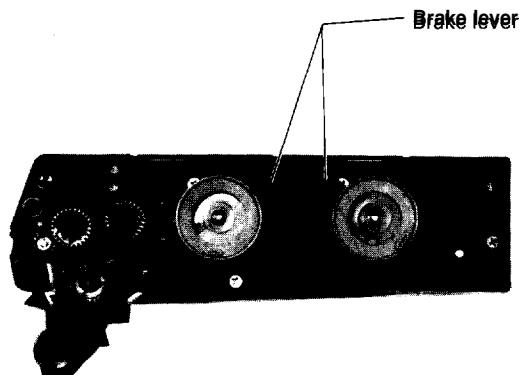


Fig. 3-37 Removal of brake lever

c) Removal of selection and feed units 1 and 2.

There are two bin selectors, the red unit operates bin 1, the blue unit operates bin 2. Each unit can be removed by taking out one E-ring and pulling outward from the pickup roller shaft. Remove the flat washer located between the unit and frame.

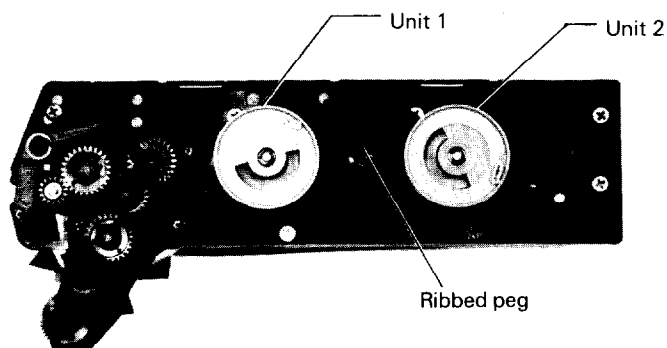


Fig. 3.38 Removal of selection and feed units 1 and 2

d) Remove the gear wheel.

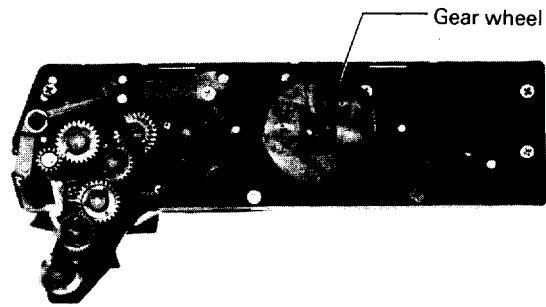


Fig. 3.39 Removal of gear wheel

e) Turn the pickup roller bearing counterclockwise to remove it. To remove the pickup roller: first pull the pickup roller to the left and take out the right shaft; then, lift it out.

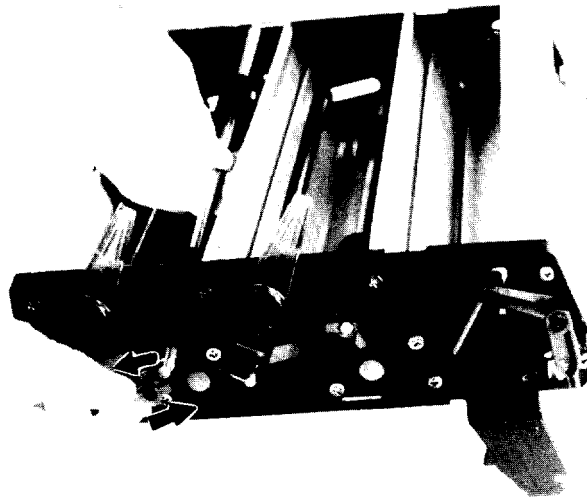


Fig. 3.40 Removal of pickup roller

(4) Removal of the pressure shaft

Remove the E-ring attached to the gear of either the left or right side, and take the pressure shaft out of the frame.

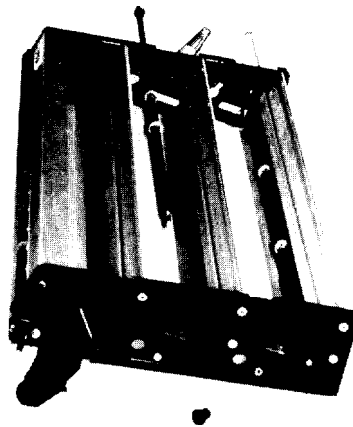


Fig. 3.41 Removal of the pressure shaft

(5) Removal of the output selector and eject roller shaft

- a) Remove the spring located between the output selector arms of the left and right sides and the frame.
- b) Remove the left and right output selector arms.

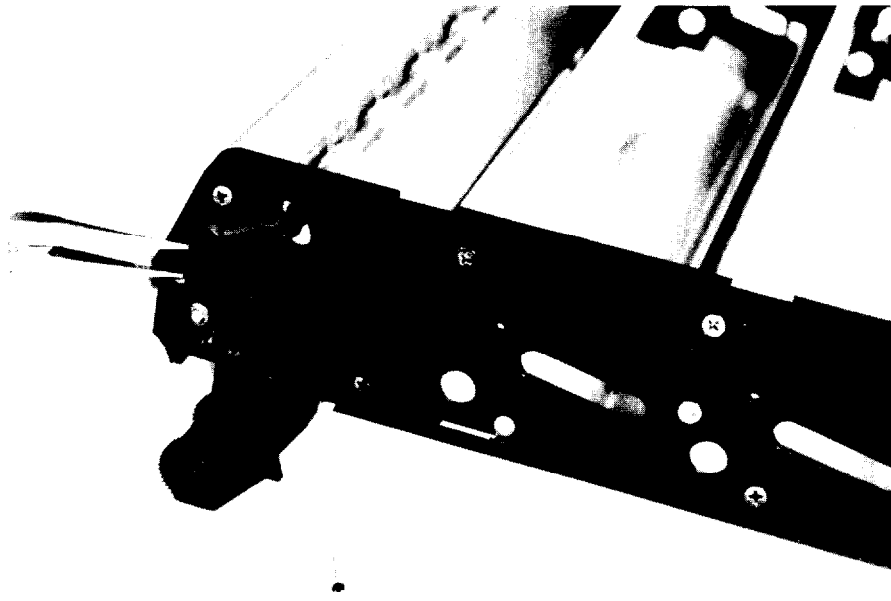


Fig. 3.42 Removal of output selector arms

- c) Remove left and right screws securing profile 0, and remove the profile.
- d) To remove the front eject roller shaft 0, grasp the left and right side and pull forward.
- e) Remove the output selector 0.

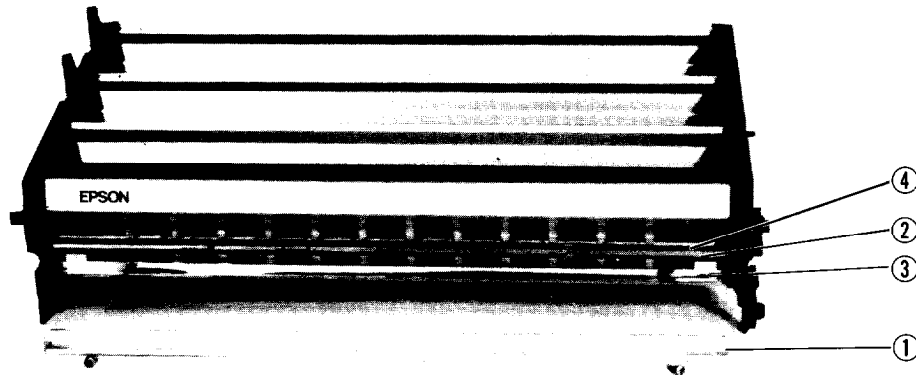


Fig. 3.43 Removal of profile, eject roller shaft, output selector

- f) Release the plastic tabs at either side of the rear eject roller shaft; then, grasp the shaft at each end and pull forward to remove it.

(6) Removal of the printer adapter

a) Removing the printer adapter (left side)

Remove the three M4.2 x 19 screws securing the printer adapter and remove it.

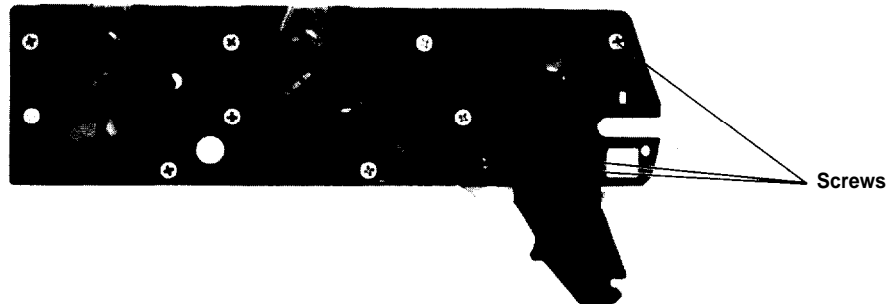


Fig. 3.44 Removal of the printer adapter (left)

b) Removing the printer adapter (right side)

Remove the three M4.2 x 19 screws securing the right side of the printer adapter and remove it.

c) Removing the gear wheels

The gear wheel attached to the printer adapter (right side) is secured with the snap-in type gear lock. Pry the gear lock off with a flat bladed screw driver.

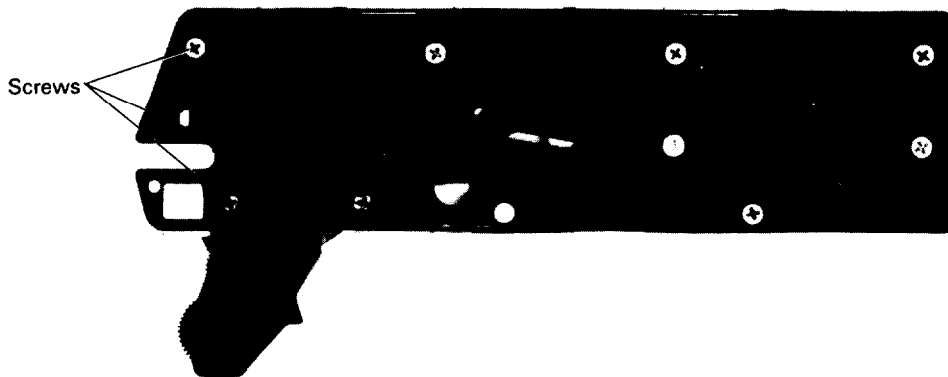


Fig. 3.45 Removal of the printer adapter (right), gear wheels

3.4.4.2 Assembly

The procedure for assembling the cut sheet feeder #8334/8344 is described in this section. The procedure is basically the reverse to that for disassembly. Some points requiring special attention are explained below.

Caution: Make sure that each reassembled part works normally at every step of the procedure before going on to the next step.

(1) Mounting the output selector and eject roller shaft

Before mounting the output selector, be sure that each of the separator's film tabs is positioned correctly. Each double sided tab should be positioned so that the front profile is grasped between the two sides of the tab ①.

If the film is not correctly partitioned, paper may missfeed.

Mount the front eject roller shaft making sure that the gear end of the shaft is on the left.

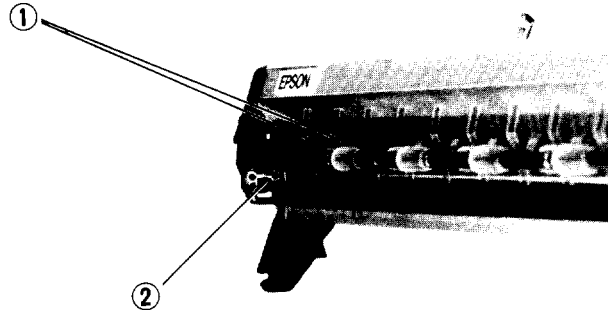


Fig. 3.46

Make sure that both ends of the output selector fit in the output selector arm groove ②.

(2) Mounting the pressure shafts

Be sure to mount the pressure shafts parallel to each other. As the rollers provided at both ends of the shaft work also as gears, be sure that they are properly engaged on the gear rails. The shaft rolls back and forth on the gear rail; however, it is most easily mounted by letting it rest in the rear position on the rail.

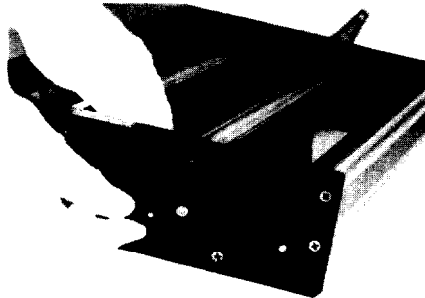


Fig. 3.47

The red rings on the pressure shaft are designed for facilitating movement of wider paper, or paper placed in a horizontal position, through the platen assembly. The rings are interchangeable and may be replaced facing in either direction.

(3) Mounting the pickup roller, gear wheel, selection and feed units 1 and 2 and brake levers.

- a) The left and right pickup rollers are interchangeable. However, in double bin units, front and rear rollers should never be intermixed. Lack of uniformity in wear on the rollers will cause paper misfeed. **Always** replace rollers as a set.
- b) When mounting the gear wheel face outward the side of the wheel with the digit engraved on it.

Front or bin 1 is red, and
Rear or bin 2 is blue.

Caution: Be sure to correctly position the red and blue bin selectors. It is possible to interchange, the red and blue selectors since each fits on the others shaft. When the red selector has been misplaced and the paper load switch is depressed, no paper will be fed through the platen assembly.

Do not forget to insert a washer between the bin selector and frame. After the selectors are mounted, rotate the assembly one full turn clockwise and then counterclockwise to make sure that it rotates smoothly.

If the unit rotation is not smooth, refer to section 3.4.5, Troubleshooting, Fault of selection and feed unit (Ref. page 3-56), and mount it again on the pickup roller.

- d) Mount the right and left brake levers correctly so that the brake slip surface makes contact with the catch plate outside frame of the selector. The side of the brake lever with the rib is the outside.

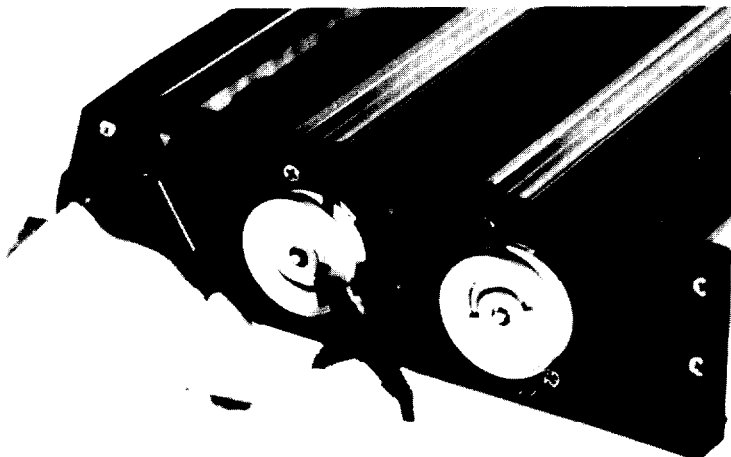


Fig. 3.48

(4) Mounting the Paper Guides and Pressure Plates

For mounting the paper guides and pressure plate, pull the release lever to the front and secure the pressure shaft. First, mount the left and right paper guides of bin 2 (rear position) and then, the left and right pressure plates.

Next, mount the left and right paper guides of bin 1 (front position) and the left and right pressure plates.

Notes:

1. If the mounting order is wrong, the left pressure plate of bin 2 (rear position) cannot be mounted.
2. The paper guide clamp should be securely pressed to the end.
3. Make sure the spring between the retaining arm and paper guide is not disengaged.
4. The paper guide should be correctly set so that the lower part of the guide covers the rib on the outside of the pickup roller.
5. Take care not to confuse the left and right paper guides..

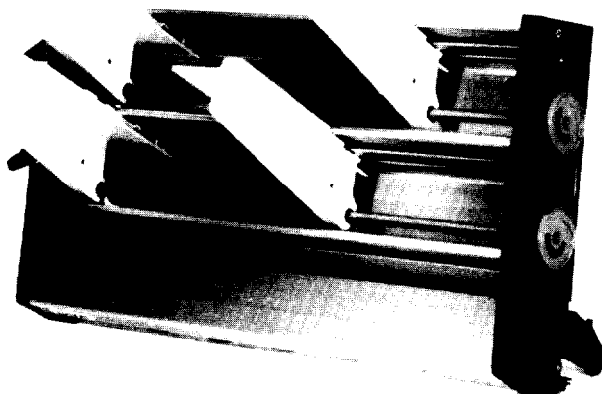


Fig. 3.49

3.4.5 Troubleshooting

3.4.5.1 General

This chapter describes troubleshooting for the cut sheet feeder #8334/8344. All the operations of the cut sheet feeder are mechanical, and each part can be actually moved and checked visually. This makes troubleshooting very easy. Perform troubleshooting by referring to 3.3.4, “Disassembly and Assembly”.

3.4.5.2 Troubleshooting procedure

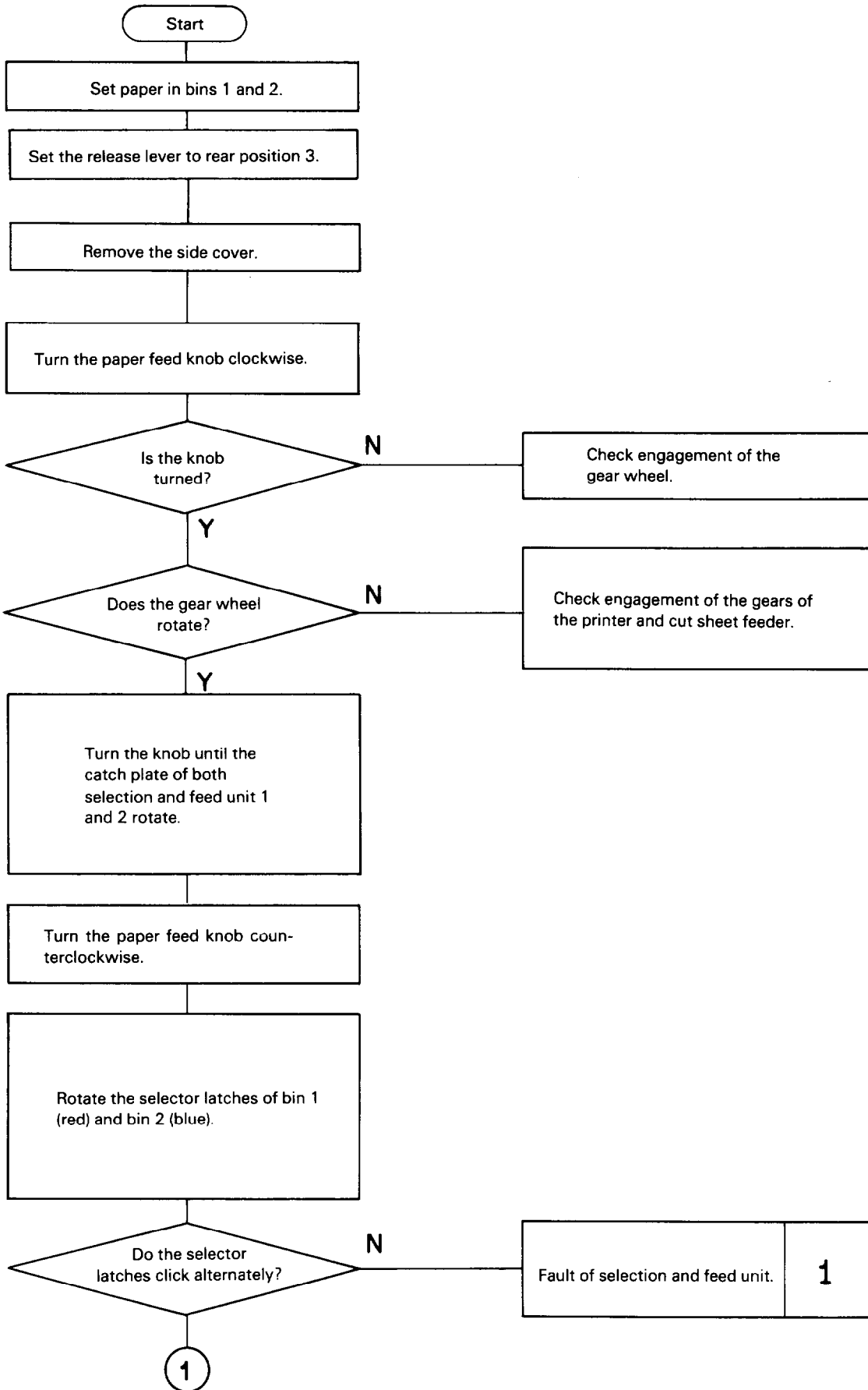
The troubleshooting procedure following consists of a two part check of component functions. The first step is to evaluate whether malfunction is caused by incorrect assembly; the second step is to see whether the problem may be traced to a defective component.

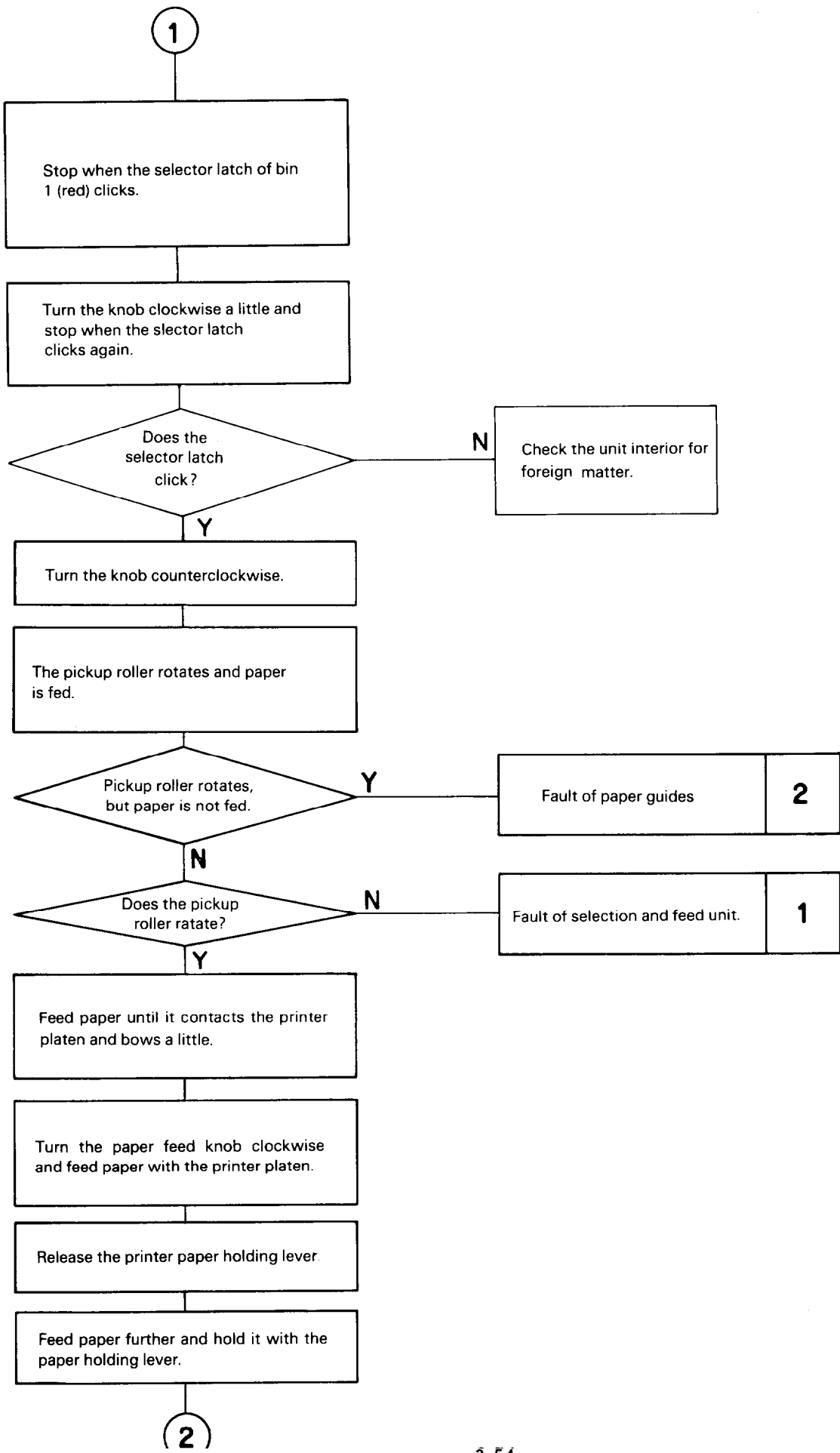
Caution: Remove the cut sheet feeder from the printer before performing any repair procedure.

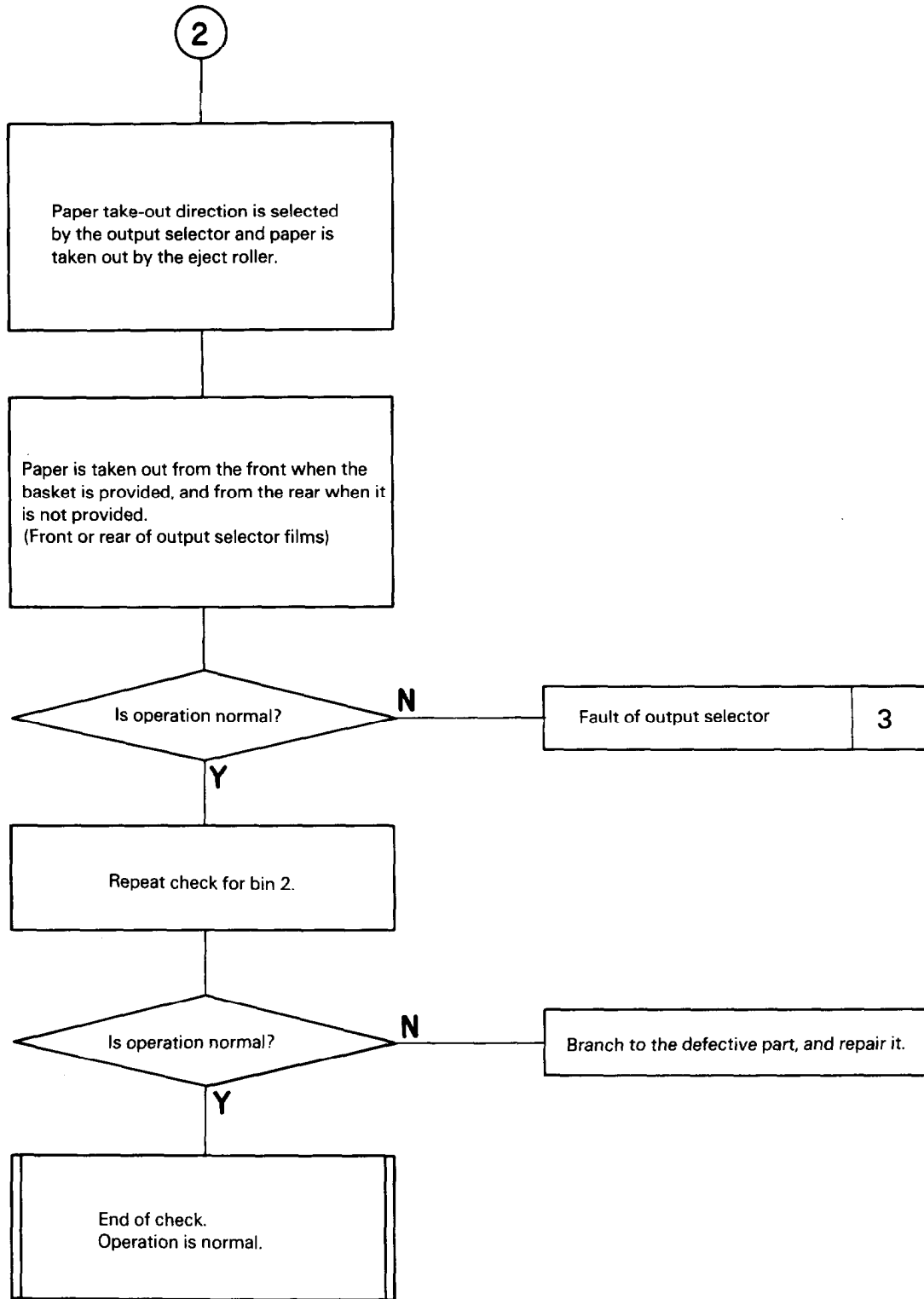
Note : Some parts must be replaced as a set (e.g., paper feed rollers). Carefully follow the instructions given in the following flow chart.

[Checking operation of the whole unit]

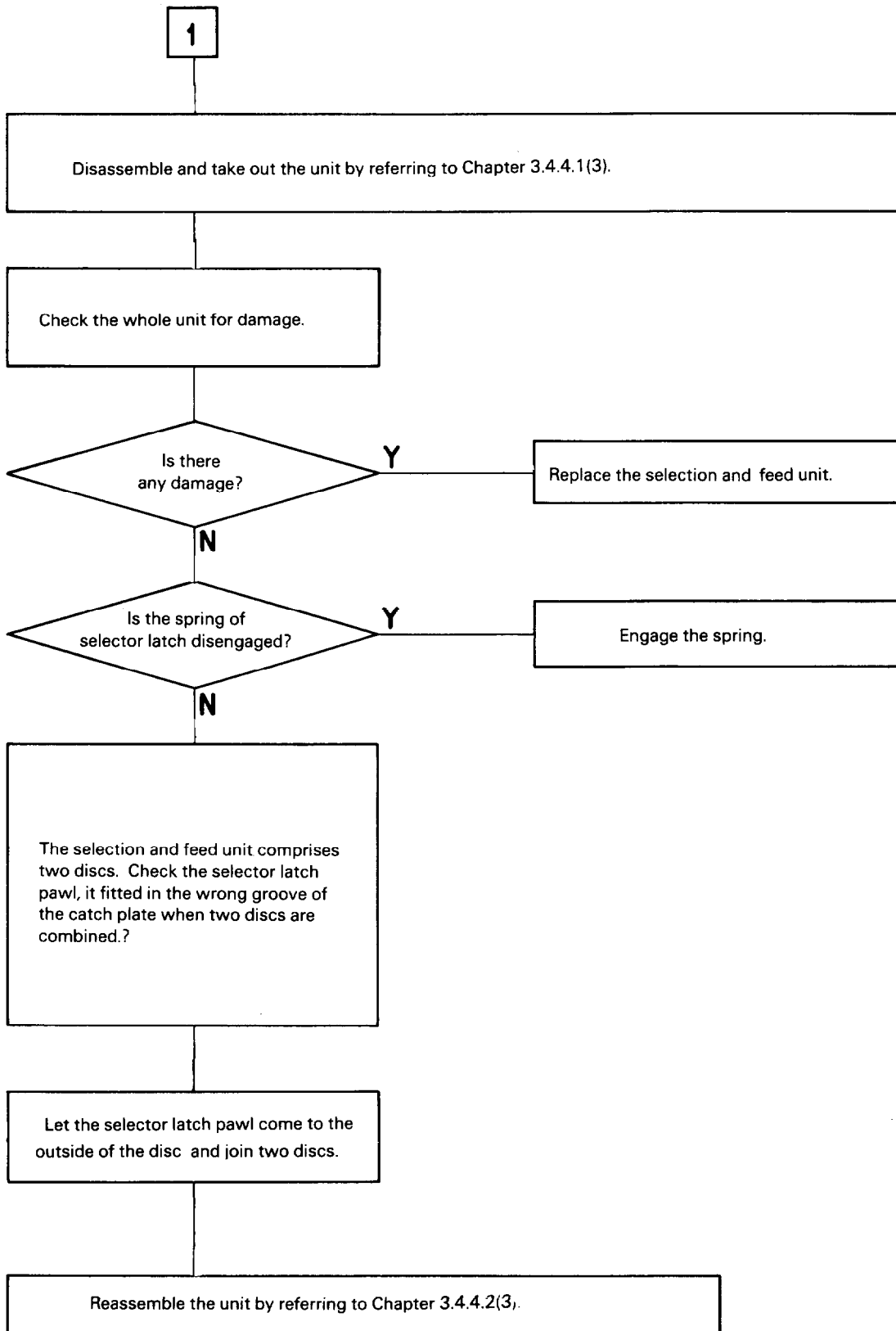
Check operation by manual operation with the Cut Sheet Feeder mounted on the printer.



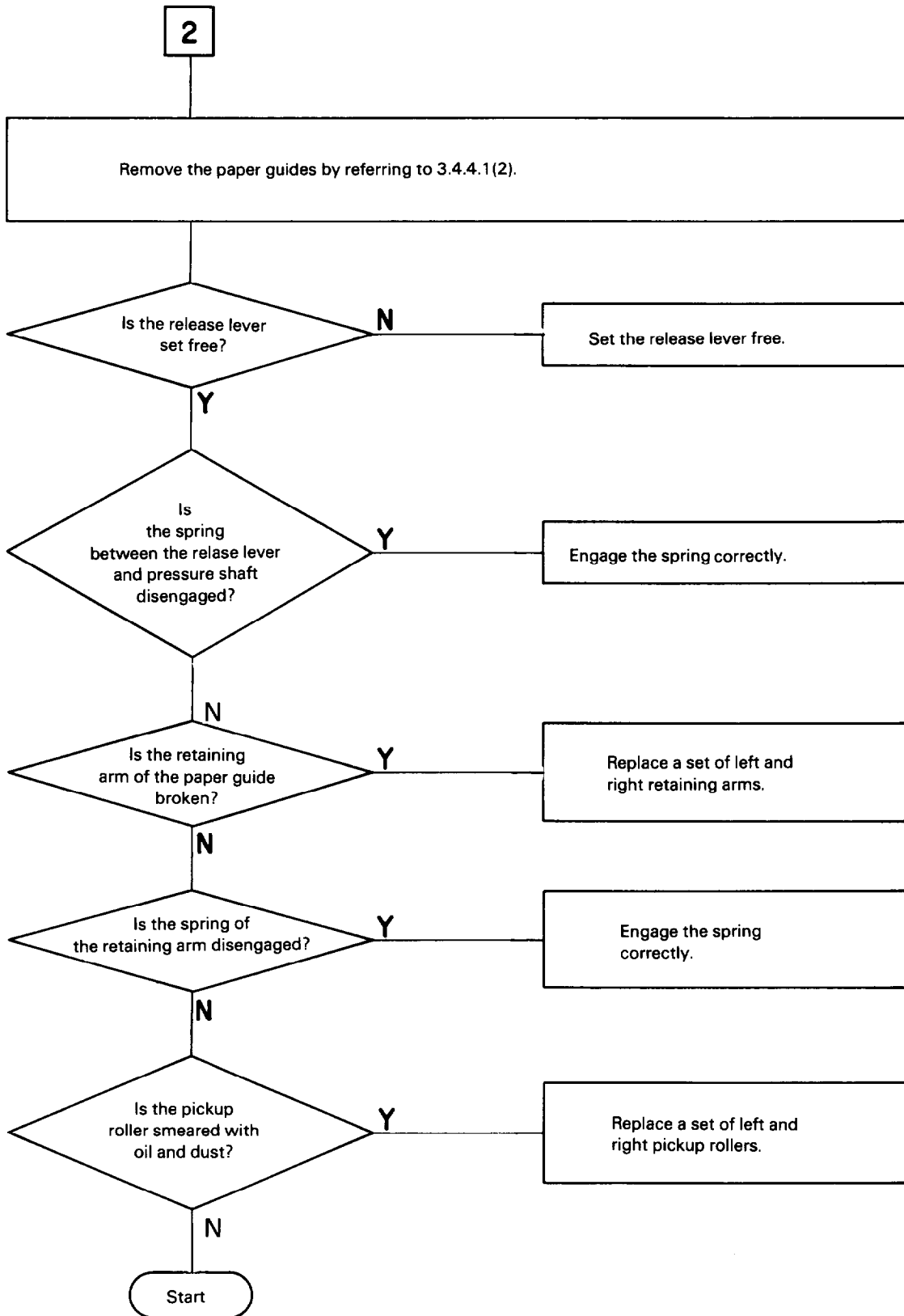




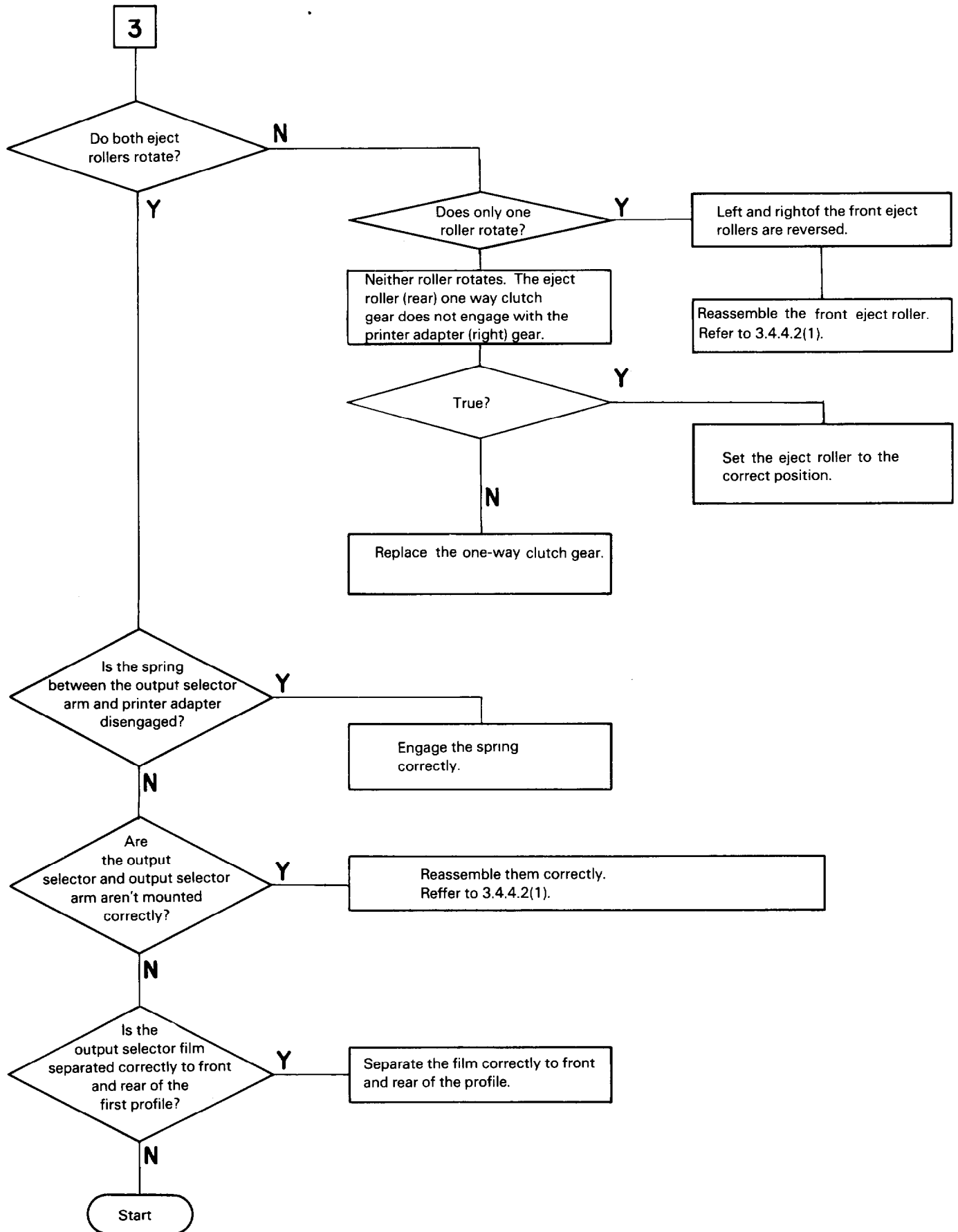
[Fault of selection and feed]



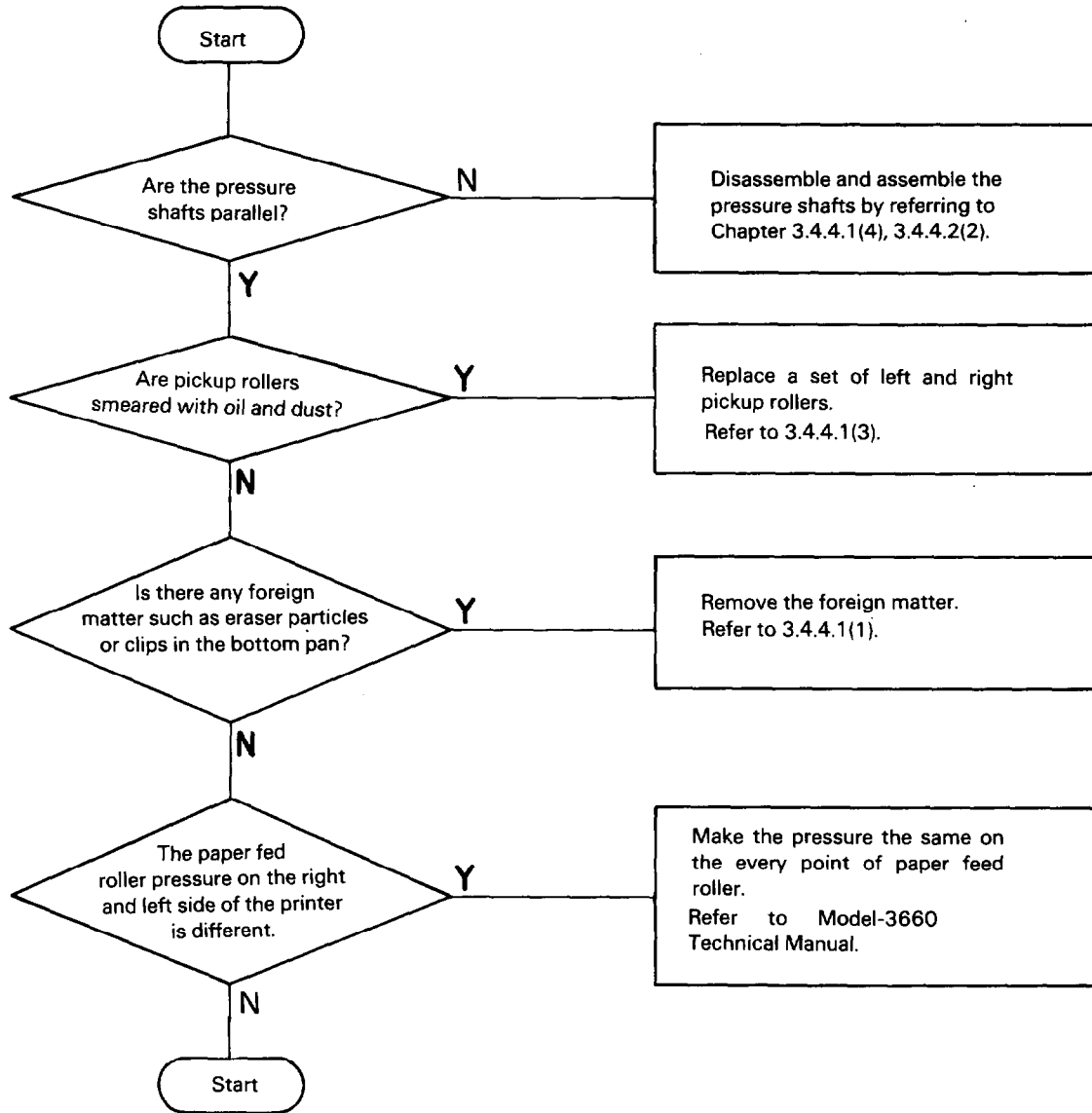
[Fault of paper guides1



[Fault of output selector]



[Other faults/Paper is fed at an angle]



3.4.6 Preventive maintenance

3.4.6.1 Introduction

Due to its proven design all models of the cut sheet feeder family require a minimum of preventive maintenance.

To provide highly reliable, trouble-free operation of the cut sheet feeder the recommended preventive maintenance procedures should be performed approximately every 6 months or 1000 hours of use, whichever comes first.

It is recommended, that during each inspection of the host printer (host machine) the cut sheet feeder device should also be functionally tested.

The preventive maintenance should include:

- General cleaning of the device,
- Checking the mechanical functions.

The cleaning of the pinch rollers and the pick-up rollers necessary at regular intervals, can be carried out by the operator after suitable instruction. Intervals are determined by the operating time and the paper type being used (Paper dust accumulation varies with the quality of the paper.)

3.4.6.2 Tools and gages required

Brush, soft

Platen cleaner MULTIPLI (Fedron Platen Cleaner)

Cloth, lint-free

Vacuum cleaner

Precautions:

- We recommend platen cleaner MULTIPLI or its equivalent as cleaning agent. Unsuitable cleaning agents harden rubber and eventually result in paper feed problems.
- Typical platen cleaners are flammable and have a very low flashpoint.
- Do not use platen cleaner to clean plastic parts. Most plastic parts can be damaged by typical platen cleaners. Use alcohol to clean plastic parts.

3.4.6.3 General cleaning of the cut sheet feeder

To remove the side covers and expose the drive mechanism for cleaning.

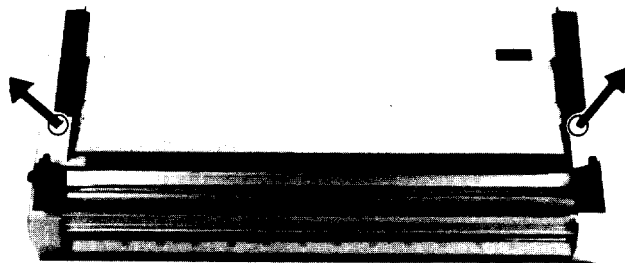


Fig. 3.50 Remove the side covers from the Feeder

Pull outward on the side covers as shown in figure 3-50.

3.4.6.4 Cleaning procedure

- Remove all paper dust from the feeder, using a vacuum cleaner with a small nozzle.
- Brush all paper dust from the eject rollers.
 - Ensure, that the paper deflector is not damaged or loose.
- Check the surface of the eject rollers. If one or more of the rollers are damaged, the complete shaft must be replaced.
- Clean all rubber rollers (pick-up rollers) with MULTIPLI platen cleaner.
- Check the surface of all rubber rollers (pick-up rollers.)
 - Damaged rubber rollers will cause registration problems.
 - If one of the pick-up rollers is damaged or unevenly worn, both rollers must be replaced.

Caution!

Regularly check the pick-up roller shafts, the eject roller shafts, and the gear wheels for wear or damage.

Clean the following three parts as necessary:

- Clean the DELRIN bushes of the eject roller shaft with denatured alcohol.
- Clean the studs of all gear wheels with denatured alcohol.
- Check the function of the “selection and feed unit”.
 - Ensure, that the selector latch operates freely, clean it with denatured alcohol as required. (Do not use oil or grease.)

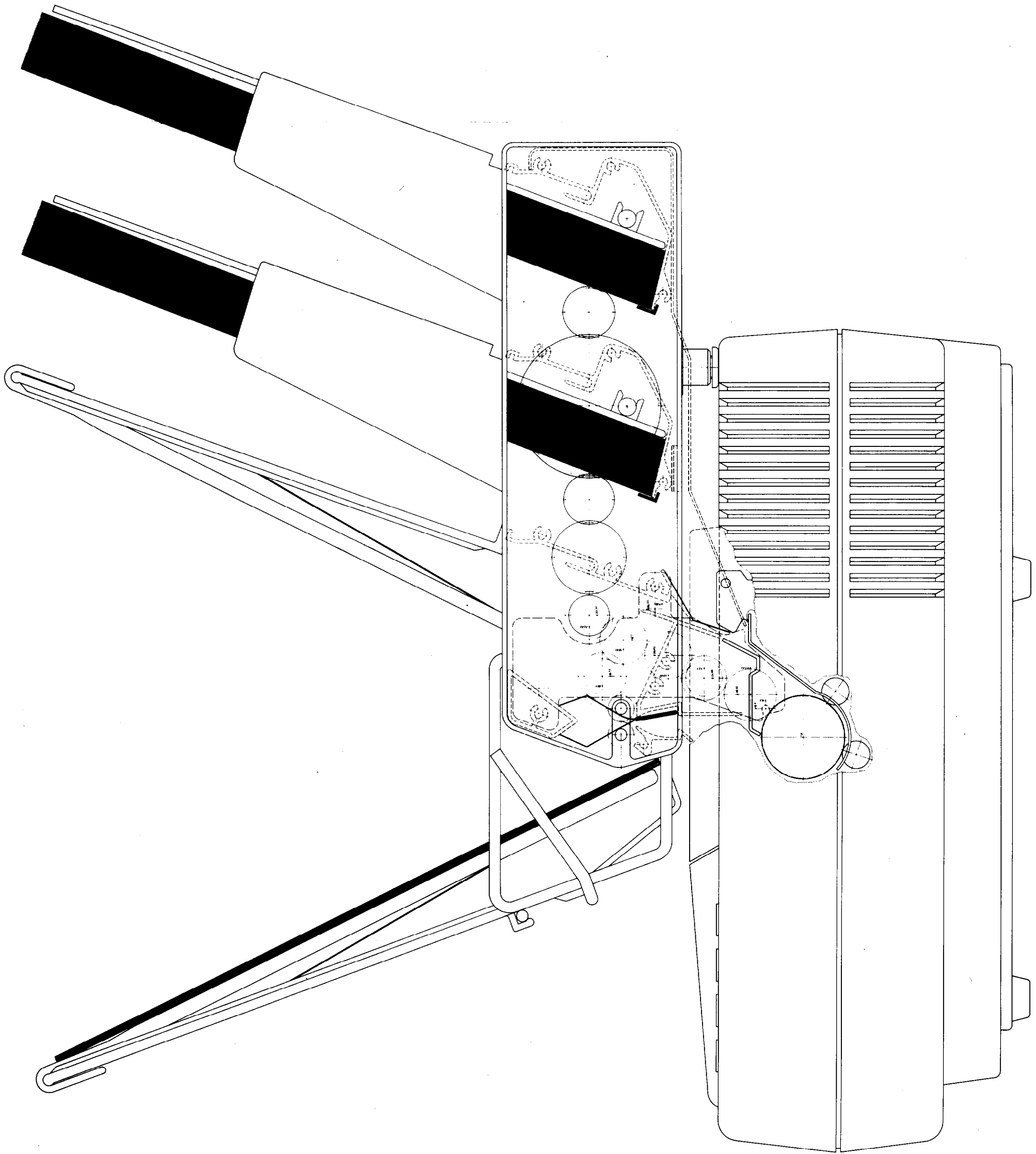
Caution!

The following parts contain a one-way clutch:

Catch plates of the “selection and feed unit”

Gear wheels

DO NOT CLEAN THIS ONE-WAY CLUTCHES WITH DENATURED ALCOHOL



CHAPTER 4

DISASSEMBLY/ASSEMBLY AND ADJUSTMENT

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4.1 General

This chapter describes the method of disassembling the LQ-1500 Terminal Printer for replacement of major components.

4.2 Tools and Measuring Instruments

The tools and measuring instruments contained in Tables 4.1 and 4.2 of this section must be prepared by the user prior to disassembling and troubleshooting the LQ-1500. Under the column "Class" in Table 4.2 code "A" denotes the tool or measuring instrument mandaton/ for maintenance and repair of the printer, whereas code "B" denotes the tool or measuring instrument not necessarily essential but recommended to facilitate such maintenance and repair.

Table 4.1 List of tools

Tool No.	Tool	Remarks
B741400100	Brush for lubrication # 1	○
B741400200	Brush for lubrication # 2	○
B741600100	Brush for cleaning	○
B740400100	Round nose plier	○
B741000100	Tweezers	○
B740200100	Soldering iron	○
B740800200	Retaining plier # 1.5	○
B740800400	Retaining plier # 2.5	○
B740800500	Retaining plier # 3	○
B740800600	Retaining plier # 4	○
B740800700	Retaining plier # 5	○
B740800800	Retaining plier # 6	○
B740801000	Retaining plier # 8	○
B743000100	(-) Driver	○
B743800200	(+) Driver # 2	○
B776700301	Thickness gauge (0.5 mm)	ⓔ
B747700300	Tension gauge (2000 gr)	○
B741700200	Hexagonal box driver	○
B740101100	Torque driver (26 kg)	○
B740101302	(+) Bit # 2 (100 mm)	○

○: Commercially available

ⓔ: EPSON tool

Table 4.2 List of measuring instruments

Name of Tool	Specification	Class
Oscilloscope	50 MHz	A
Tester		A
Multimeter		B
Logic state analyzer		B

Lubricants and adhesive List

The lubricants and adhesive which are indispensable for maintenance and repair are given below.

Product	Designation	Supply unit	Remarks
Oil	O-2	40 cc	ⓔ
Grease	G-14	40 gr	ⓔ
Adhesive	Neji Lock # 2 (G)	1,000 gr	○

○ : Commercially available

ⓔ : Available only from EPSON

4.3 Disassembly and Assembly

The following explains the disassembly procedures of the main components. Unless otherwise specified, each disassembled component can be reassembled by reversing the disassembly process. Therefore, assembly procedure is omitted.

4.3.1 Removal of upper case (Fig. 4.1)

To check the inside of the LQ-1500, first open the upper case according to the procedure below.

- STEP 1: Remove the accessories such as the printer lid sheet guide, etc.
- STEP 2: Remove the hand paper feed knob.
- STEP 3: Remove 6 screws from the upper case. (Fig. 4.1)

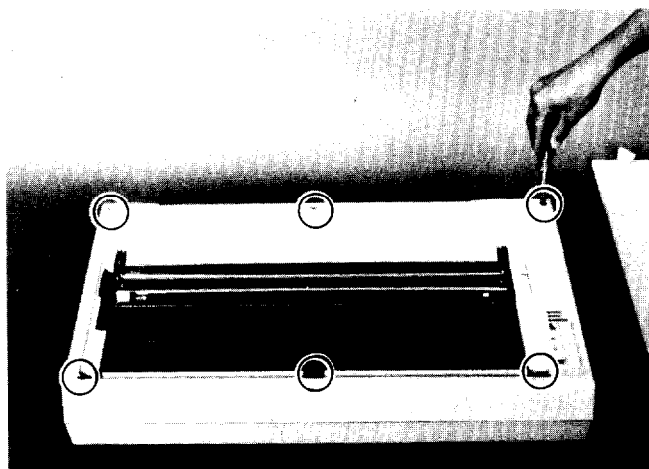


Fig. 4.1 Removal of upper case

- STEP 4: Lift the upper case, disconnect the connectors at the rear side of the control panel, then remove the upper case.

The location of each printer component with the upper case detached is as shown in Fig. 4.2.

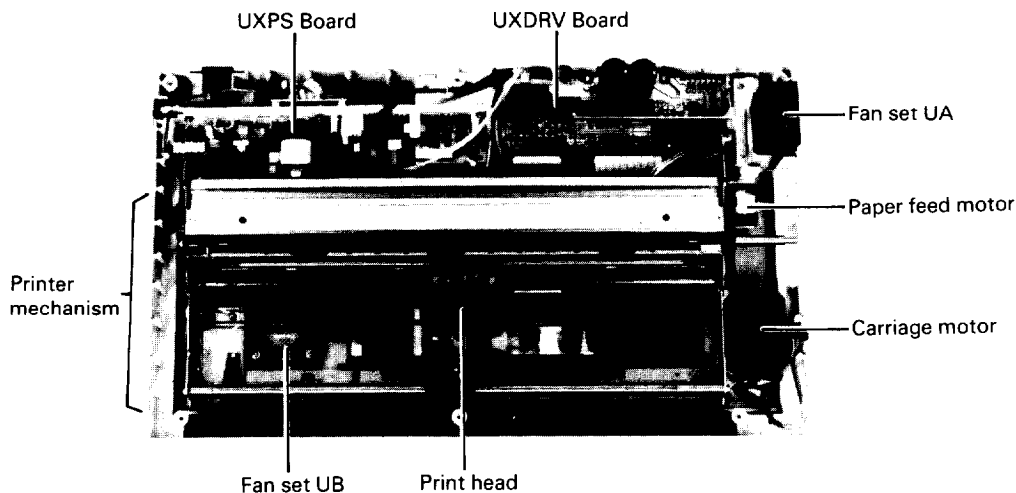


Fig. 4.2 Location of each component

4.3.2 Removing the circuit boards

The electric circuit boards in the LQ-1500, control the Model-3660 printer mechanism, and include the control circuit board (UXMCL), the driver circuit board (UXDRV), the power circuit board (UXPS or UXFIL) and an interface circuit board (IUPIF, IUIE or IURS).

The procedure for removing these boards, described below, should be followed when even replacing a circuit part.

(1) Removal of control circuit board (UXMCL)

The control circuit board, on which many parts are provided, is the center of the electric circuit boards. Removal work should be carried out with care in the following procedure:

- STEP 1: Remove the upper case. (See paragraph 4.3.1.)
- STEP 2: Remove the interface unit. (See paragraph 4.3.2 (4))
- STEP 3: Remove the printer mechanism. (See paragraph 4.3.3.)
- STEP 4: Remove the control circuit board sheet. (See Fig. 4.3.)

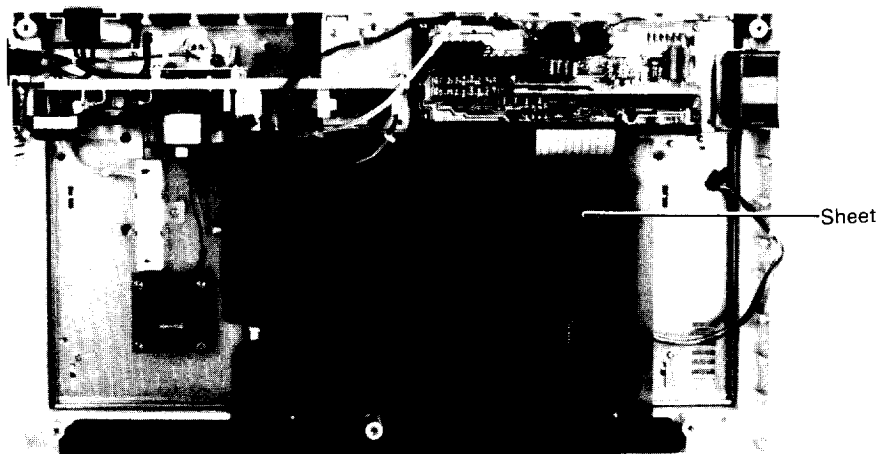


Fig. 4.3 Control circuit board sheet

- STEP 5 : Disconnect connector CN3 ① from the driver circuit board (UXDRV).
- STEP 6: Disconnect connector CN2 ② from the power circuit board (UXPS).
- STEP 7 : Remove 2 screws ③ securing the control circuit board (UXMCL).
- STEP 8: Disconnect the 9 hooks securing the control circuit board by hand, and remove it from the lower case.

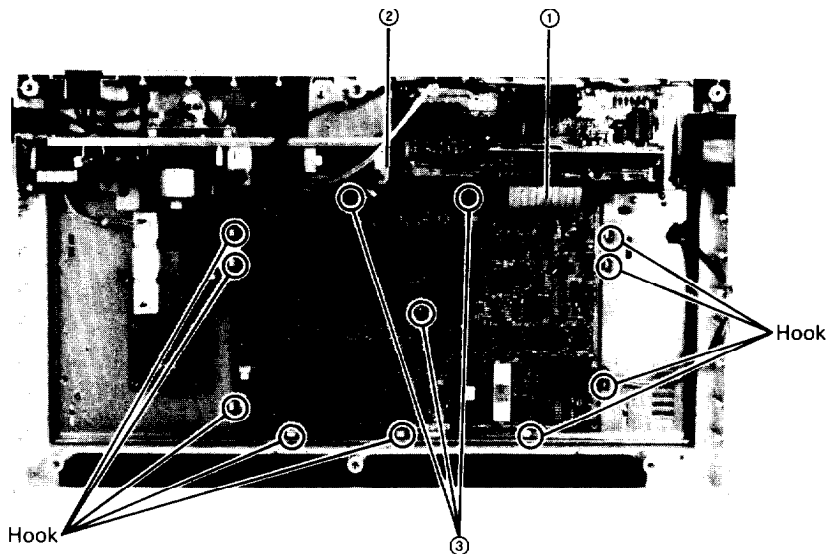


Fig. 4.4 Removal of the UXMCL board

(2) Removal of driver circuit board (UXDRV)

The driver circuit board drives the head, carriage and paper feed assemblies.

- STEP 1: Remove the upper case. (See paragraph 4.3.1.)
- STEP 2: Disconnect the connectors from the driver circuit board.
 1. Disconnect connector CN2 ①.
 2. Disconnect connector CN3 ②.
 3. Disconnect connector CN4 ③.
 4. Disconnect connector CN5 ④.
 5. Disconnect connector CN7 ⑤.
 6. Disconnect connector CN6 ⑥.
- STEP 3: Disconnect connector CN3 ⑦ from the power circuit board.

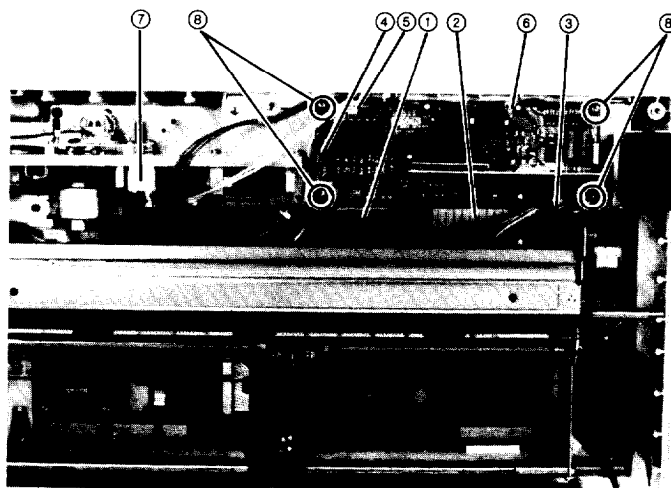


Fig. 4.5 Removal of the UXDRV board

- STEP 4: Remove 4 screws ⑧ securing the driver circuit board.

(3) Removal of power circuit board (UXPS or UXFIL)

The power circuit board supplies DC voltage to the control circuit board and the driver circuit board.

STEP 1: Remove the upper case. (See paragraph 4.3.1.)

STEP 2: Disconnect the connectors from the power circuit board.

1. Disconnect connector CN3 ①.

2. Disconnect connector CN2 ②.

3. Disconnect connector CN4 ③.

STEP 3: Remove screw ④ from the GND terminal in the AC inlet.

STEP 4: Remove 3 screws ⑤ securing the power circuit board to the base plate.

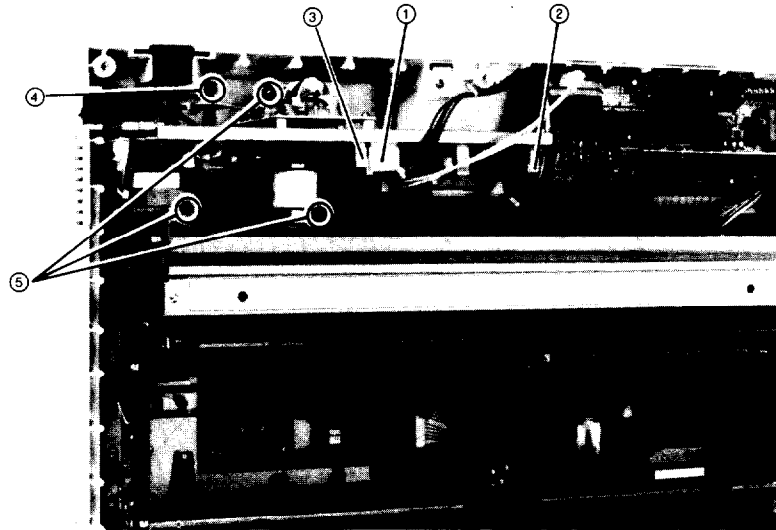


Fig. 4.6 Removal of the UXPS/UXFIL board

(4) Removal of the interface unit

The interface unit includes a chassis and one of three interface circuit boards (IUPIF, IUIE, or IURS).

STEP 1: Remove 2 screws ① securing the interface unit.

STEP 2: Remove the interface circuit board by pulling the insides of levers ② at right and left of the interface unit towards you.

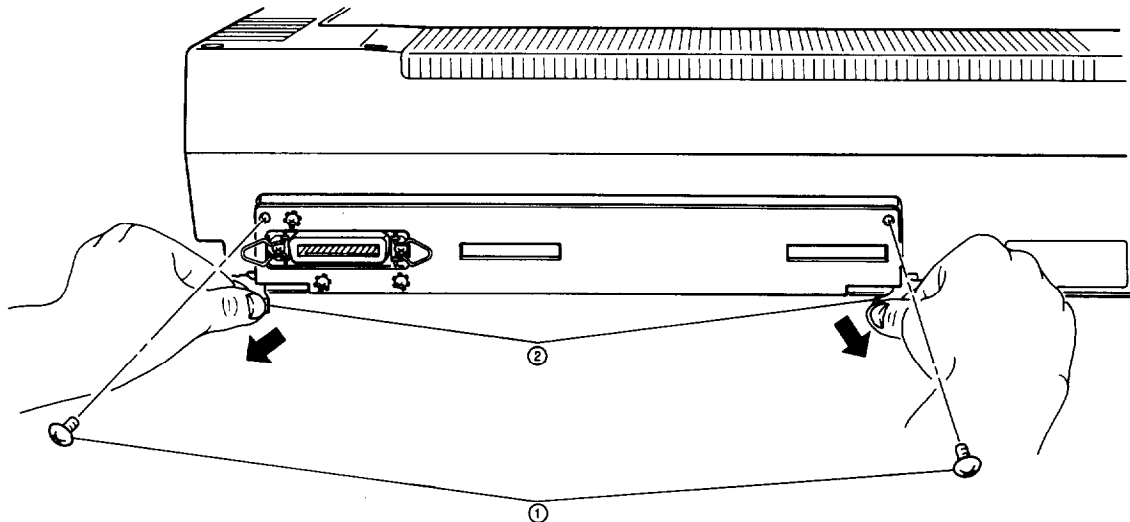


Fig. 4.7 Removal of the I/F unit

4.3.3 Removal of Model-3660 printer mechanism

The Model-3660 printer mechanism can be detached by removing the four connectors and four screws.

Notes: When remounting the mechanism, be careful not to trap the control panel cable, paying attention to routing.

- STEP 1: Remove the upper case. (See paragraph 4.3.1.)
- STEP 2: Disconnect the connectors from the driver circuit board (UXDRV).
 - 1. Disconnect connector CN2 ①.
 - 2. Disconnect connector CN4 ②.
 - 3. Disconnect connector CN5 ③.
- STEP 3: Disconnect connector CN5 ④ from the control circuit board (UXMCL).
- STEP 4: Remove four screws ⑤ securing the mechanism to the lower case.

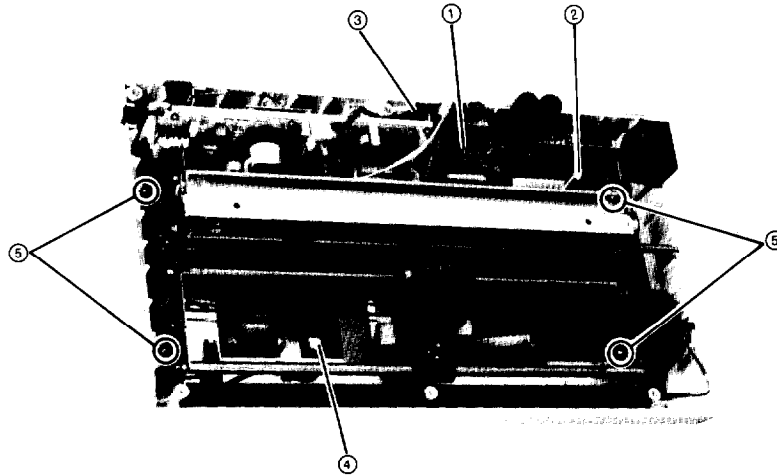


Fig. 4.8 Removal of the M-3660 printer mechanism

- STEP 5: Lift the mechanism, then remove it.

4.3.4 Removal of fan set UB (head cooling fan)

- STEP 1: Remove the upper case. (See paragraph 4.3.1.)
- STEP 2: Remove the printer mechanism. (See paragraph 4.3.3.)
- STEP 3: Disconnect connector CN4 ① from the power circuit board (UXPS).
- STEP 4: Remove 4 screws ② securing the fan set to the base plate.

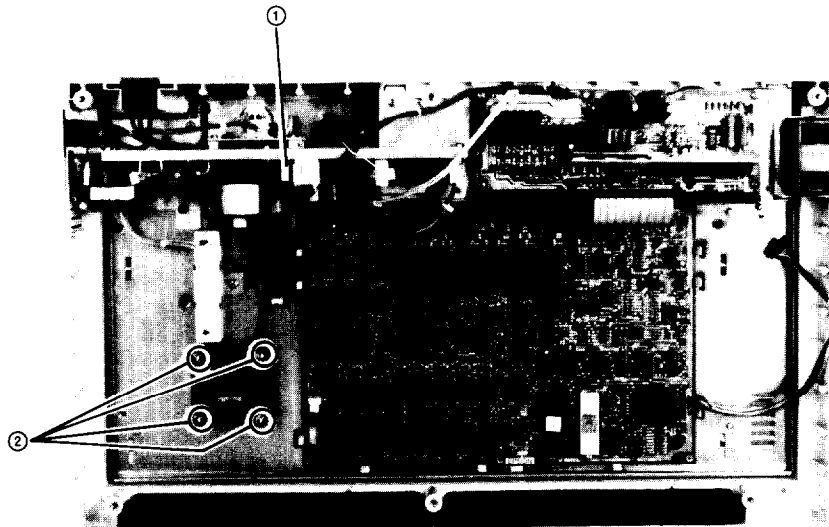


Fig. 4.9 Removal of the fan set UB

4.3.5 Removal, installation and adjustment of print head

(1) Removal of print head

Replace the print head in the following procedure:

Notes: When replacing the print head, be sure to turn off the power.

STEP 1: Remove the ribbon cassette from the print head.

STEP 2: Manually the print head fully to the left.

STEP 3: Holding the head connector section down, disconnect the connectors in order, first the right then the left with the head cables kept in a horizontal position.

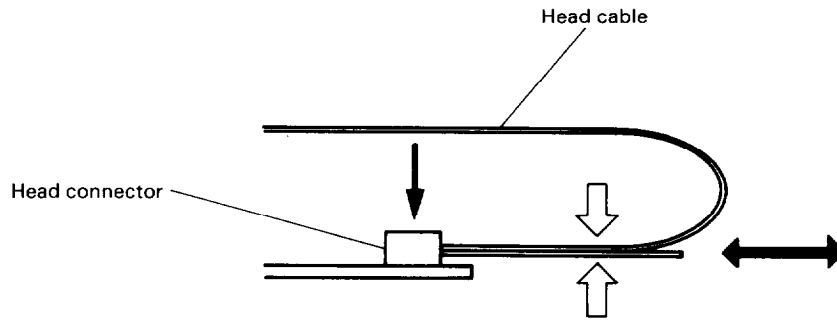


Fig. 4.10 Removal of head cable

STEP 4: Remove the print head by removing 2 screws ① securing it.

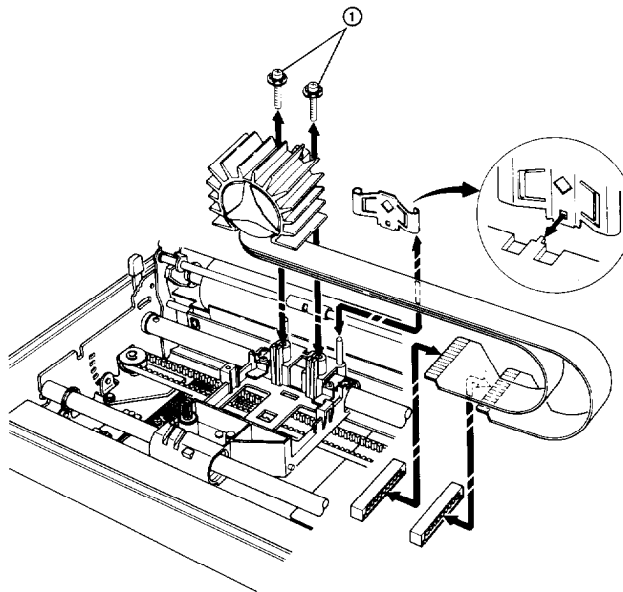


Fig. 4.11 Removal of print head

STEP 5: Remove the ribbon mask.

Note: Pull up the ribbon mask, pressing its lower center section lightly.

(2) Installation and adjustment of print head

STEP 1: Set the adjusting lever to the first step.

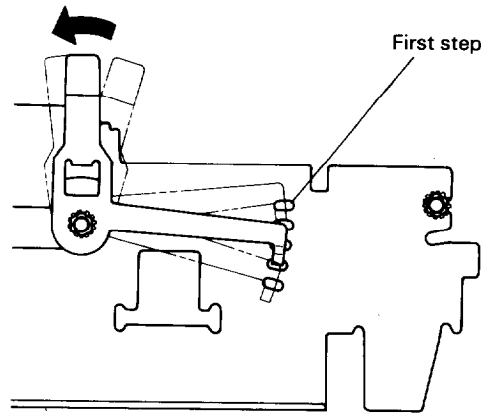


Fig. 4.12 Adjusting lever

STEP 2: Secure the print head by 2 screws.

STEP 3: Connect 2 head cables to the connectors on Model-3660 in order from left to right.

Caution: Unless head cables are securely connected, the assembly may not function.

STEP 4: Adjust the opening between the print head top and the platen to approximately 0.5 mm and tighten the 2 screws.

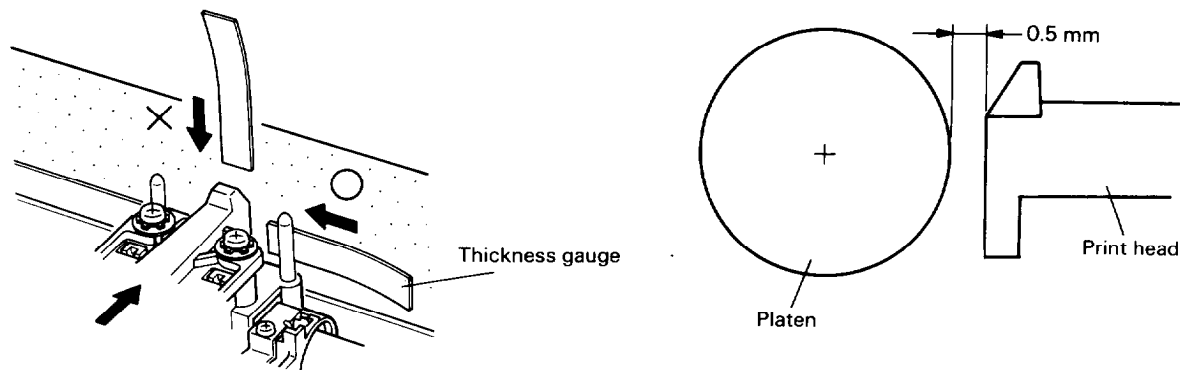


Fig. 4.13 Gap adjustment

Note: Insert the thickness gauge laterally.

STEP 5: Set the adjusting lever to the fifth step.

STEP 6 : Hook the ribbon mask in the ribbon fixing pin, and set it to the original position.

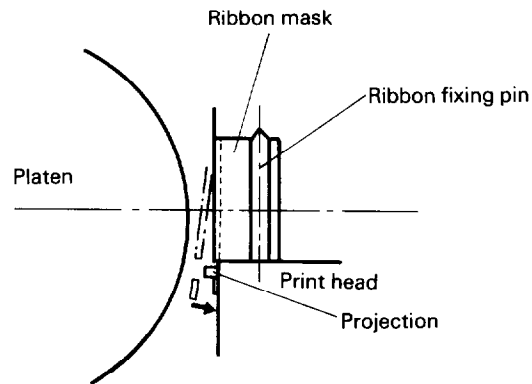


Fig. 4.14 Setting of ribbon mask

Note: Incorrect setting of the ribbon mask may cause jammed ribbon or paper.

STEP 7: Set the adjusting lever again according to the paper to be used.

4.3.6 Removal of CPU and ROM

The CPUs and ROMs are socket-connected on the UXMCL and interface circuit boards are socket-connected.

STEP 1: To remove a circuit board, follow the removal procedure in paragraph 4.3.2.

STEP 2: Remove the ROM and RAM from the board with care.

1) When replacing ROM

1)-1 Using a chip extractor, remove the chip. If extractor is not available, carefully unplug the chip, gradually loosening it.

1)-2 To replace the ROM, insert it in its socket, matching the index points (notches) which indicates pin 1 on the chip and socket.

2) Removal of CPU (40 PINS TYPE LSI)

2)-1 Follow instructions for removal of the ROM.

2)-2 When inserting CPU on the IC socket, insert it carefully using the insertion tool.

Note: Be carefull not to damage pins of CPU in case of the insertion and the removal.

4.3.7 Adjustment of the print alignment (backlash)

1. Location of SW1

Dip switch 1 is located on the UXMCL circuit board as shown in Fig. 4.15; it is possible to set SW1 without removing other components.

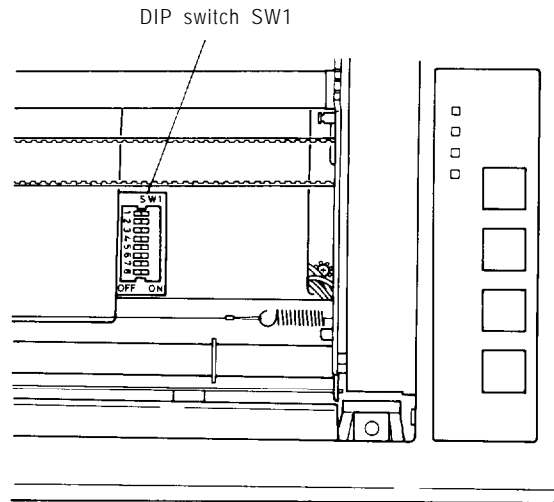


Fig. 4.15 Location of SW1

2. Position and function of SW1

(1) SW1-1/SW1-2

Table 4.3 below defines the results of each switch setting combination when the print direction is right to left in the low speed printing mode.

Table 4.3 Setting of SW1 -1 /SW1 -2

Pattern	SW1-1	SW1-2	Functions
0	ON	ON	Delay 1/180" (Shift to right)
1	OFF	ON	Keep on standard
2	ON	OFF	Move 1/180" (Shift to left)
3	OFF	OFF	Move 2/180" (Shift to left)

(2) SW1-3/SW1-4

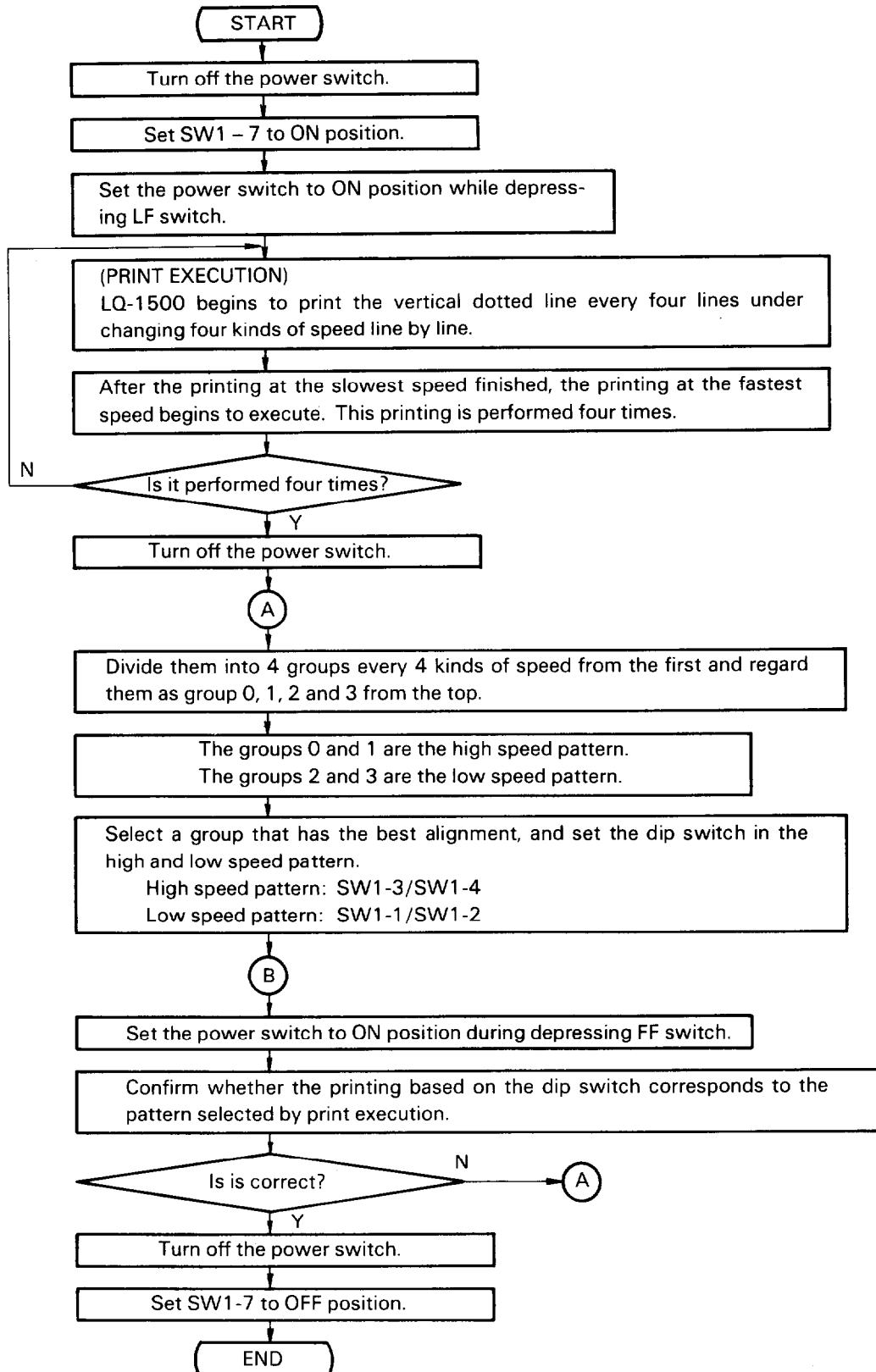
Table 4.4 below defines the results of each switch setting combination when the print direction in the right and left.

Table 4.4 Setting of SW1 -3/SW1-4

Pattern	SW1-3	SW1-4	Functions
0	ON	ON	Delay 1/120" (Shift to right)
1	OFF	ON	Keep on standard
2	ON	OFF	Move 1/120" (Shift to left)
3	OFF	OFF	Move 2/120" (Shift to left)

3. Adjustment

It is necessary to adjust the printing backlash when the print alignment on one line becomes bad. This adjustment is performed by starting the test program of ROM with the operation of dip switch SW1. Please adjust step by step according to the following flow chart.



4.4 Adjustment

4.4.1 MTS and DTS sensor board adjustment

Adjust the MTS sensor board if sensor board has changed.

Special Tools: Synchroscope

Extension cables (2 types)

- STEP 1: Turn off the power.
- STEP 2: Remove the upper case.
- STEP 3: Remove the printer mechanism.
- STEP 4: Remove the UXDRV board.
- STEP 5: Connect the extension cable
- STEP 6: Scope set:
 - CH1: MTS signal (One side of resistance R35 on the UXMCL board)
 - TIME: 200 μ set
- Note: Resistance R35 is near the IC '5C'.
- STEP 7: Turn off Dip switch 2 - 7 on the interface board so that it is in DRAFT mode.
- STEP 8: Set the paper and execute self-print-test. Check the following waveform.

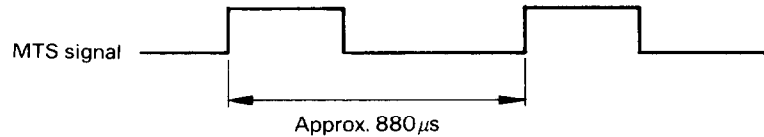


Fig. 4.16 MTS

- STEP 9: If the waveform is not the same as above, go to stop 10.
If the waveform is same as above, then skip to STEP 13.
- STEP 10: Loosen the setscrew (CP(P) M2.5 x 4) of the MTS sensor board.
- STEP 11: Move the PTS sensor board in the direction of the arrow to adjust T1 cycle to be almost equal for both travel courses.

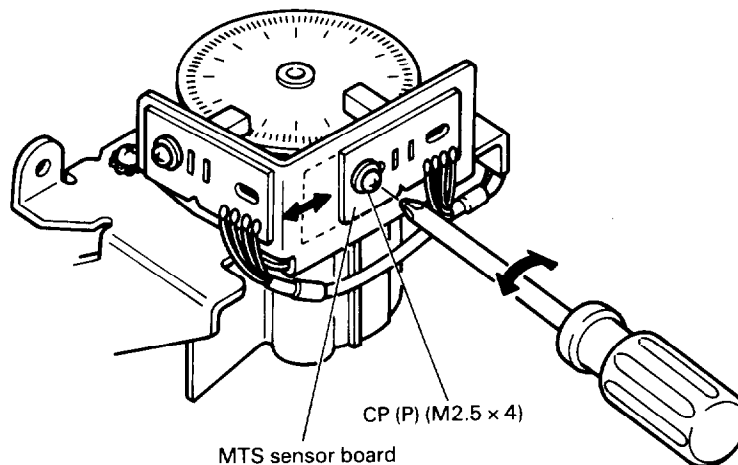


Fig. 4.17 Adjustment of the MTS sensor position

STEP 12: Securely tighten the setscrew if adjustment has completed.

STEP 13: Adjust the phases of MTS and DTS signals.

Scope set:

CH1: MTS signal (One side of resistance R35 on the UXMCL Board)

CH2: DTS signal (One side of resistance R34 on the UXMCL Board)

TIME: 200 usec CHOP mode

TRIG: CH1

STEP 14: Execute the self-print-test and check the following waveforms.

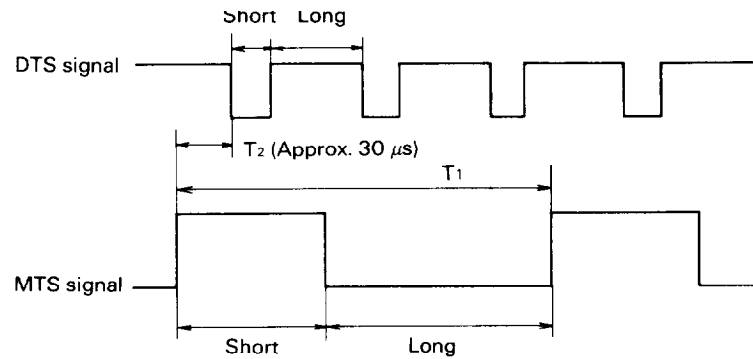


Fig. 4.18 MTS/DTS timing

STEP 15: If DTS signal is not same as above, continue to next step.

If DTS signal is same as above, timing adjustment is correct.

STEP 16: Loosen the setscrew (CP(P) M2.5 x 4) of the DTS sensor board.

STEP 17: Move the DTS sensor board in the direction of the arrow to adjust T2 cycle to be almost equal for both travel courses.

(Standard value of T2 cycle for both travel courses: Within 20 us)

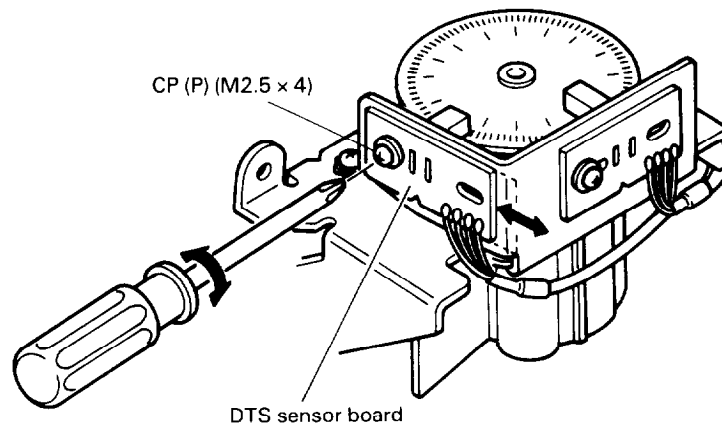


Fig. 4.19 Adjustment of the DTS sensor position

STEP 18: Securely tighten the setscrew.

STEP 19: Turn off the printer power.

STEP 20: Disconnect the extension cable and assemble the UXDRV board and the printer mechanism to lower case of the printer.

STEP 21: Return the DIP switch (DIP 2 - 7) to previous setting.

STEP 22: Attach the upper case.

4.4.2 H.P. sensor board adjustment (Figs. 4.20,4.21)

Disconnect the printer from the power source before making the adjustment.

(Adjustment of the printing start position)

Adjust the H.P. sensor board if sensor board has changed.

STEP 1: Execute the MTS sensor board adjustment from STEP 1 through STEP 5 (Section 4.4.1).

STEP 2: Set the printing paper, and print more than 7 or 8 lines. (Print "H" characters)

STEP 3: Loosen the setscrew (CP (P) M3 x 6) of the H.P. sensor board.

STEP 4: Move the H.P. sensor board in the direction of the arrow, and align so that the scale shaft graduations comes to the center of the letter.

If adjustment has been completed. Go to step 5.

Note: Turn the switch to off each time, and adjust.

STEP 5 : Confirm the phase of MTS and DTS signals when this adjustment has been performed.

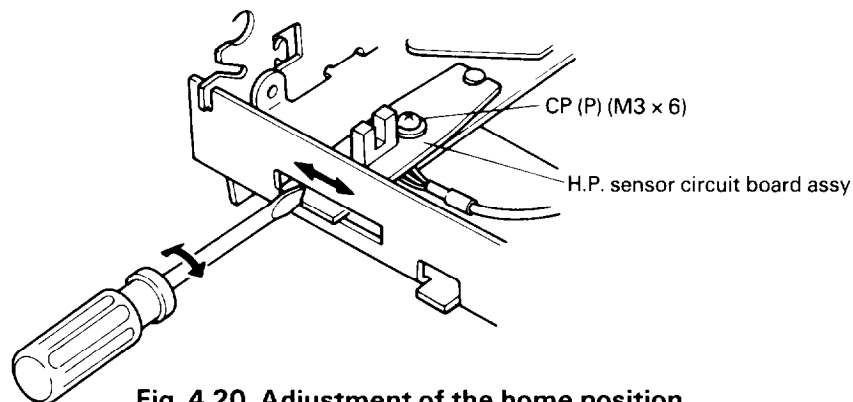


Fig. 4.20 Adjustment of the home position

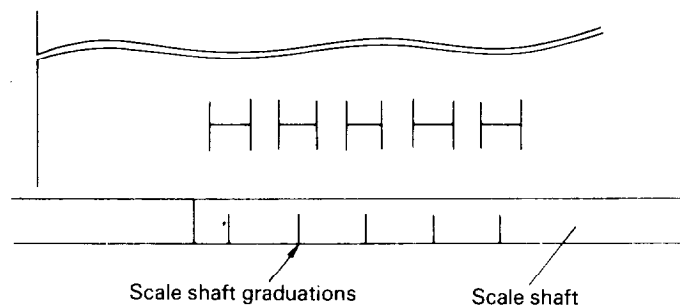


Fig. 4.21 Character position

STEP 6 : Scope set;

CH 1: MTS signal

CH2: H.P. signal

TIME: 200 ,usec CHOP mode

Execute printing and confirm the waveform.

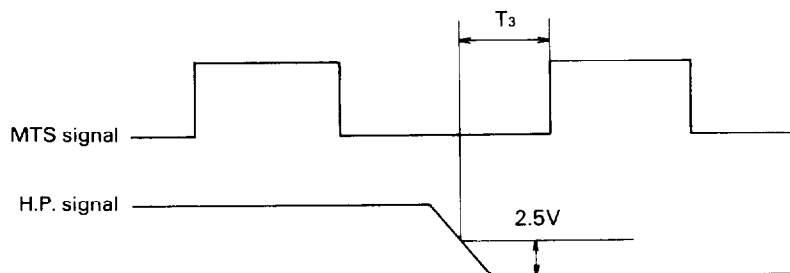


Fig. 4.22 Home position timing

- STEP 7:** Move and adjust the H.P. sensor board so that T3 reaches 300 to 600 us just before the adjustment is performed.
- STEP 8:** Securely tighten the setscrew.
- STEP 9:** Confirm that the sensor of the H.P. sensor board and sensor interception plate of the carriage do not contact with each other when the adjusting lever is set at the highest or lowest level.

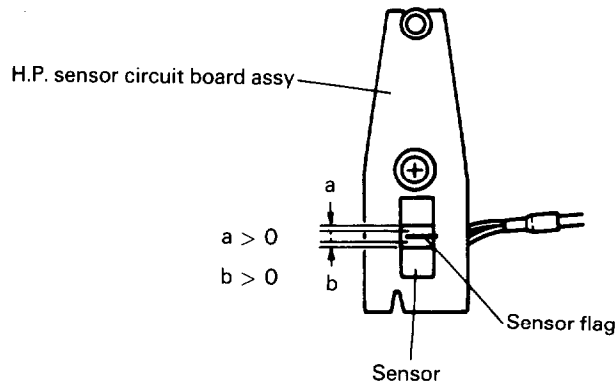


Fig. 4.23 H.P. sensor

4.4.3 Backlash of the carriage motor and belt driving pulley (Fig. 4.24)

If print alignment with both directional print is bad, adjust the backlash.

- STEP 1:** Loosen the setscrews (CPO M3 x 6) which tighten the carriage motor frame and carriage motor mounting plate.
- STEP 2:** Adjust the backlash between the motor pinion of the carriage motor and the belt driving pulley.
(Standard value: 0.05 to 0.15 mm)
- 1) Adjust the backlash by moving the carriage motor.
 - 2) Confirm the backlash at three points during one rotation of the belt driving pulley.
- STEP 3:** Securely tighten the setscrews (CPO M3 x 6).

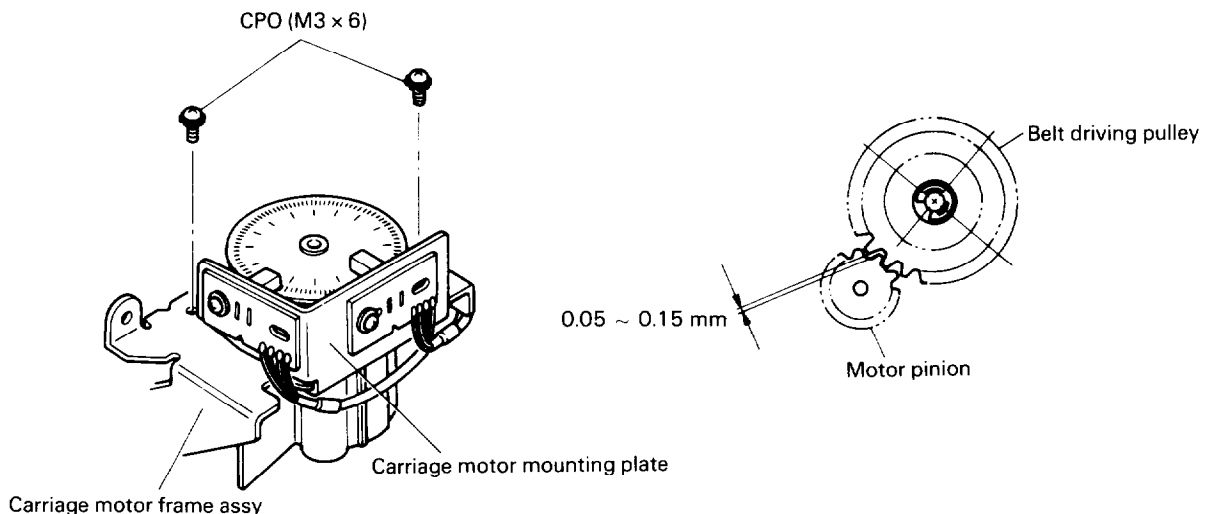


Fig. 4.24 Backlash of the carriage motor

4.4.4 Backlash of the paper feed motor and paper feeding reduction gear (Fig. 4.25)

If line spacing is unstable, adjust the backlash.

STEP 1: Loosen the setscrews (CPO M3 x 6) of the line feed motor.

STEP 2: Adjust the backlash between the motor pinion of the pulse motor and the paper feeding reduction gear.

(Standard value: 0.05 to 0.15 mm)

1) Adjust the backlash by the paper feeding reduction gear.

2) Confirm the backlash at three points during one rotation of the paper feeding reduction gear.

STEP 3: Securely tighten the setscrews (CPO M3 x 6).

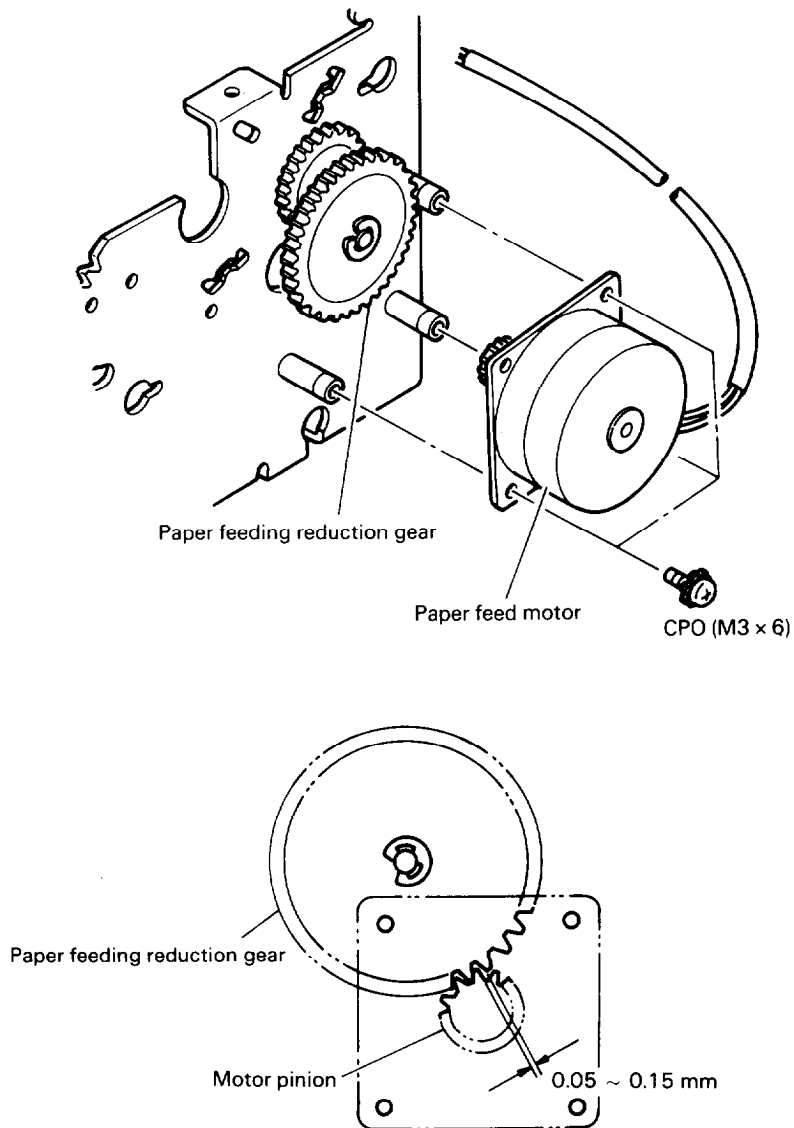


Fig. 4.25 Backlash of the paper feed motor

CHAPTER 5

TROUBLESHOOTING

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5.1 Entry to Troubleshooting

Troubleshooting is not an easy process since troubles can happen in various sections in various forms. The approach represented by the following three procedures, however, assures you of an easy entry to repair.

1. Check-out procedure (5.2)

Use: The check-out procedure provides entry to repair for troubles whose nature is not clear enough.

Level : Repair is made by unit replacement. Those with basic knowledge of machinery can perform this repair.

2. Unit repair flow charts

Use: The flow charts guide you to the repair of a faulty unit on the component level.

Level : Repair is made on the component level, so that it requires a high level of mechanical knowledge and techniques.

Procedure for troubleshooting

As the first step, repair by unit replacement is performed, using the check-out procedure. Following this replacement, be sure to recheck the replaced unit to see if it is really faulty.

(This is necessary to distinguish the unit trouble from the trouble caused by the poor contact of a connector or the like.)

As the second step, defective components in a faulty unit are replaced, using the unit repair flow chart or the trouble list.

Note 1: Please disconnect AC Plug when you replace any unit.

Note 2: Checks specified on the flow charts must be performed without fail. Replacement of components or unit without such checks can permit the new components to be damaged again.

Note 3: When you have lost track of a repair procedure, be sure to return to the original entry and start the procedure over again.

Note 4: "HI/LO" in this chapter means the alternation of high level signal and low level signal.

Note 5: Don't touch ceramic resistance because it becomes hot.

Step 1

Check-out
procedure

Repair by unit
replacement

→

Step 2

Unit repair
flow chart

Repair on the
component level

The user is recommended to keep the following replacement components:

[Circuit boards]

Name of circuit board	Part number
UXFIL	Y450205000
UXPS	Y450203000
PSU 24E	Y450505000
UXMCL	Y450201000
UXDRV	Y450202000
IUPIF	Y495201000
IUIE	Y495202000
IURS	Y495203000

[Electric devices]

Name of circuit boards	Name of devices	Location	Part number
UXMCL	μ PD780C-1	2B	X400000800
	8253-5	8A	X400082530
	μ PD8255AC-5	10A	X400082550
	C42020FA	11D	Y450800801
	C41010BA	12D	Y450800802
	8259A	9A	X400082591
	E01011BA	5B	Y450801001
	M02012GA	4A	Y450800901
	μ PD416-3	2D ~ 9D 2E ~ 9E	X400104163
	27128 (LQ5 W7)	5A	Y450803101
	27128 (LQ6 W1)	6A	Y450801202
	27128 (LQ7 W1)	7A	Y450801203
UXDRV	2SD1392	Q1 ~ Q24	X303139200
	HA13007	IC1	X440170070
	STK6982	IC2	X440759820
IUPIF	μ PD8255AC-5	7A	X400082550
IURS	μ PD7810G	9B	X400078100
	μ PD8255AC-5	3A	X400082550
	2764 (FIF2)	5A	Y490802001
	μ PD4016 C/D	6A	X400040160
IUIE	μ PD7810G	10B	X400078100
	μ PD8255AC-5	3A	X400082550
	2764 (FIF2)	6A	Y490802001
	μ PD4016 C/D	7A	X400040160

[Mechanical components]

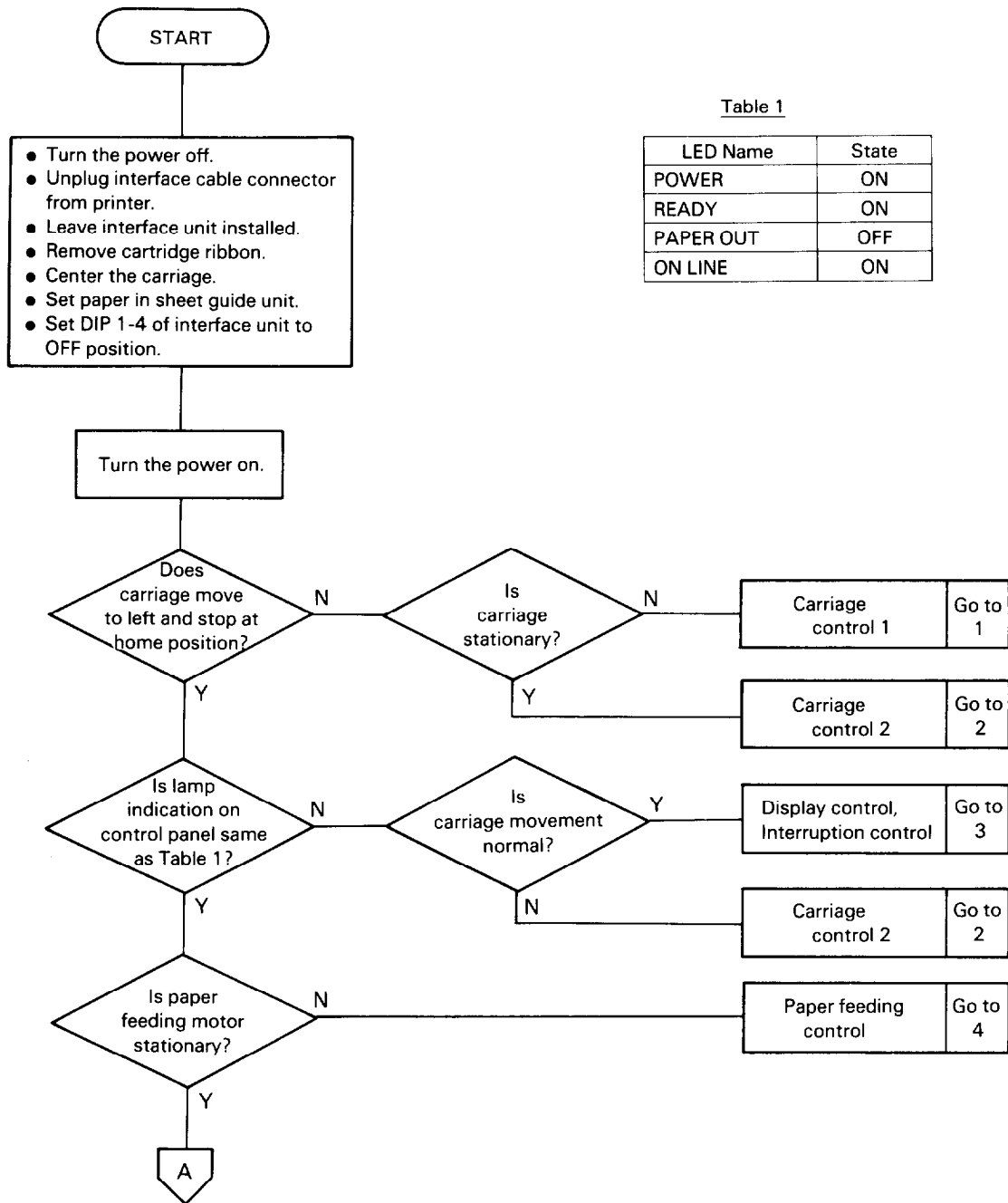
Model-3660 Y450590100

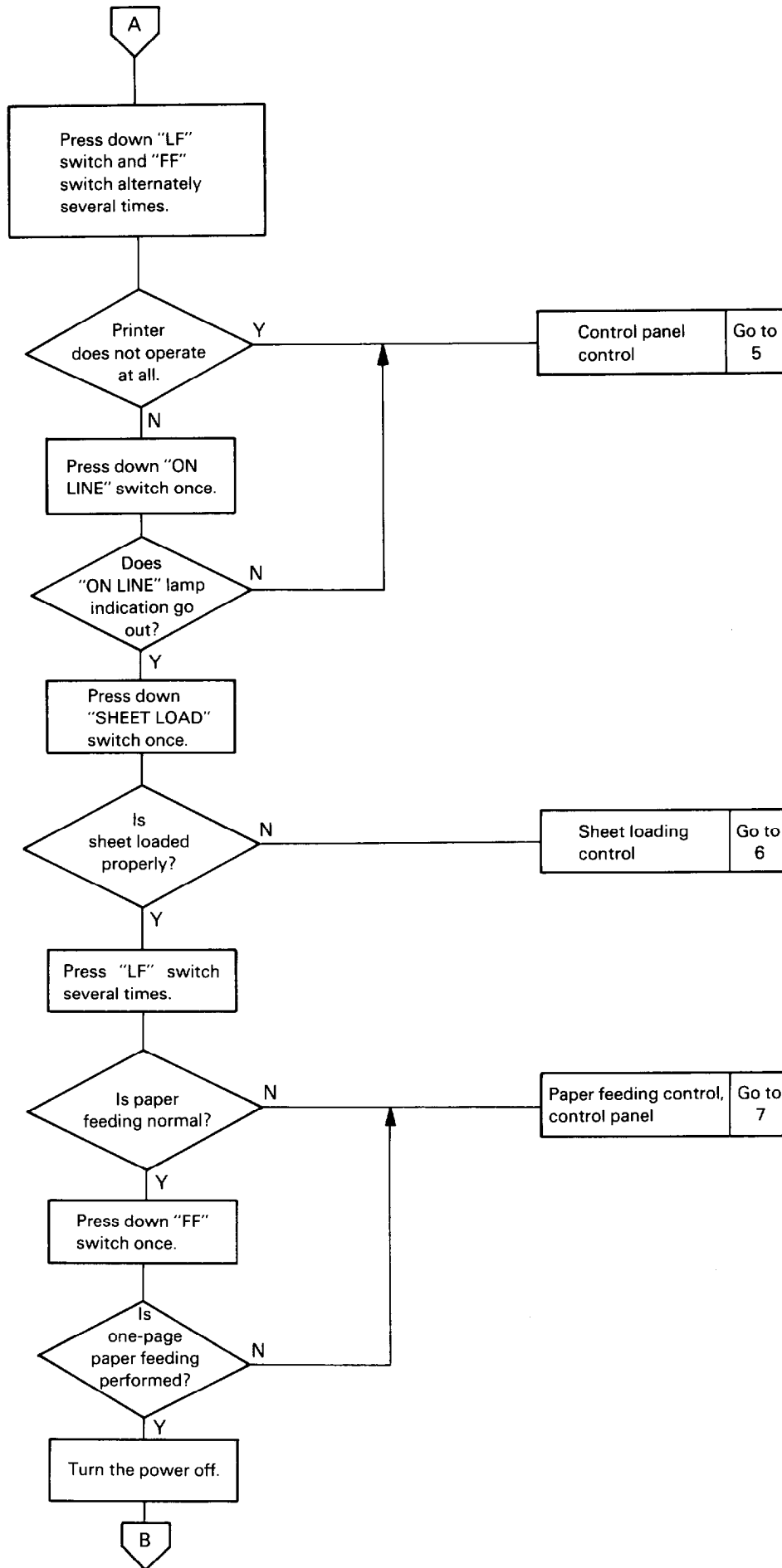
Name of part	Part number
HP sensor board assy	F318046000
PTS sensor board assy	F318030000
MTS lead	F318031000
DTS lead	F318032000
PE board assy	F318015000
Paper feeding motor assy	F318052000
Timing belt motor assy	F318027000
Ribbon mask	F318024010
Print head unit	F405100000

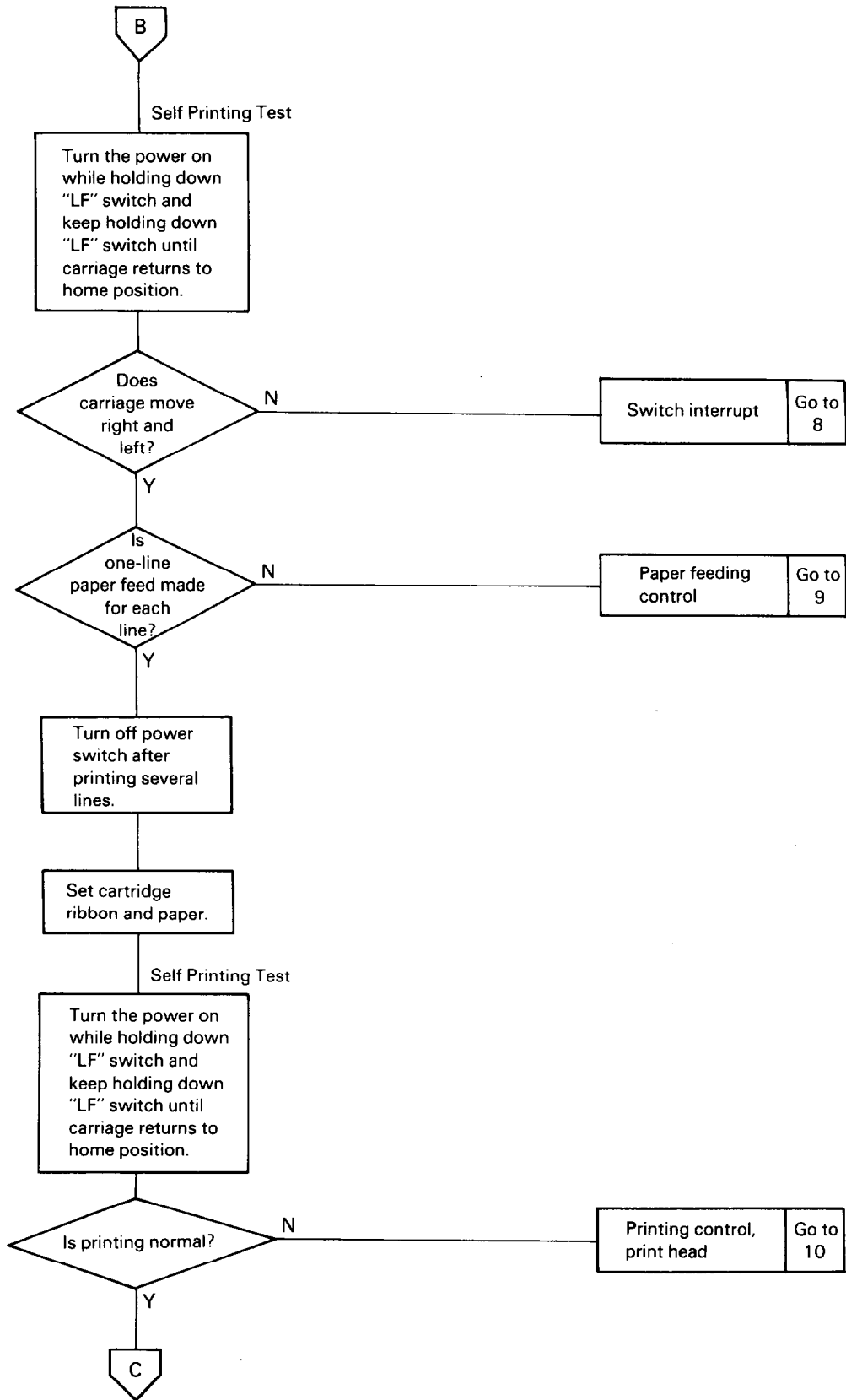
[Maintenance tool]

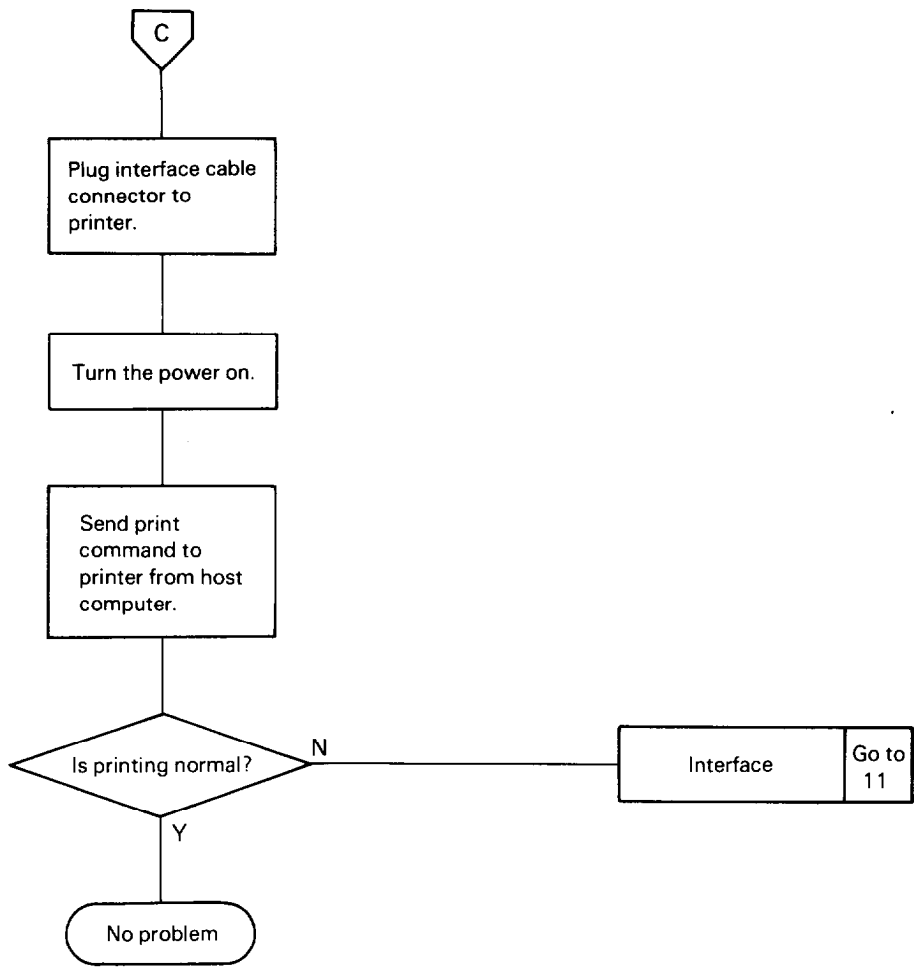
Name of tools	Number of tools
Cable set # 891 (HP sensor ↔ UXMCL)	Y450308000
Cable set # 892 (UXMCL ↔ UXDRV)	Y450309000
Cable set # 893 (UXMCL ↔ I/F unit)	Y450310000
Cable set # 894 (UXMCL ↔ UXPS)	Y450311000
Cable set # 896 (UXDRV ↔ UXPS)	Y450313000

5.2 Check-out Procedure (Repair by Unit Replacement)

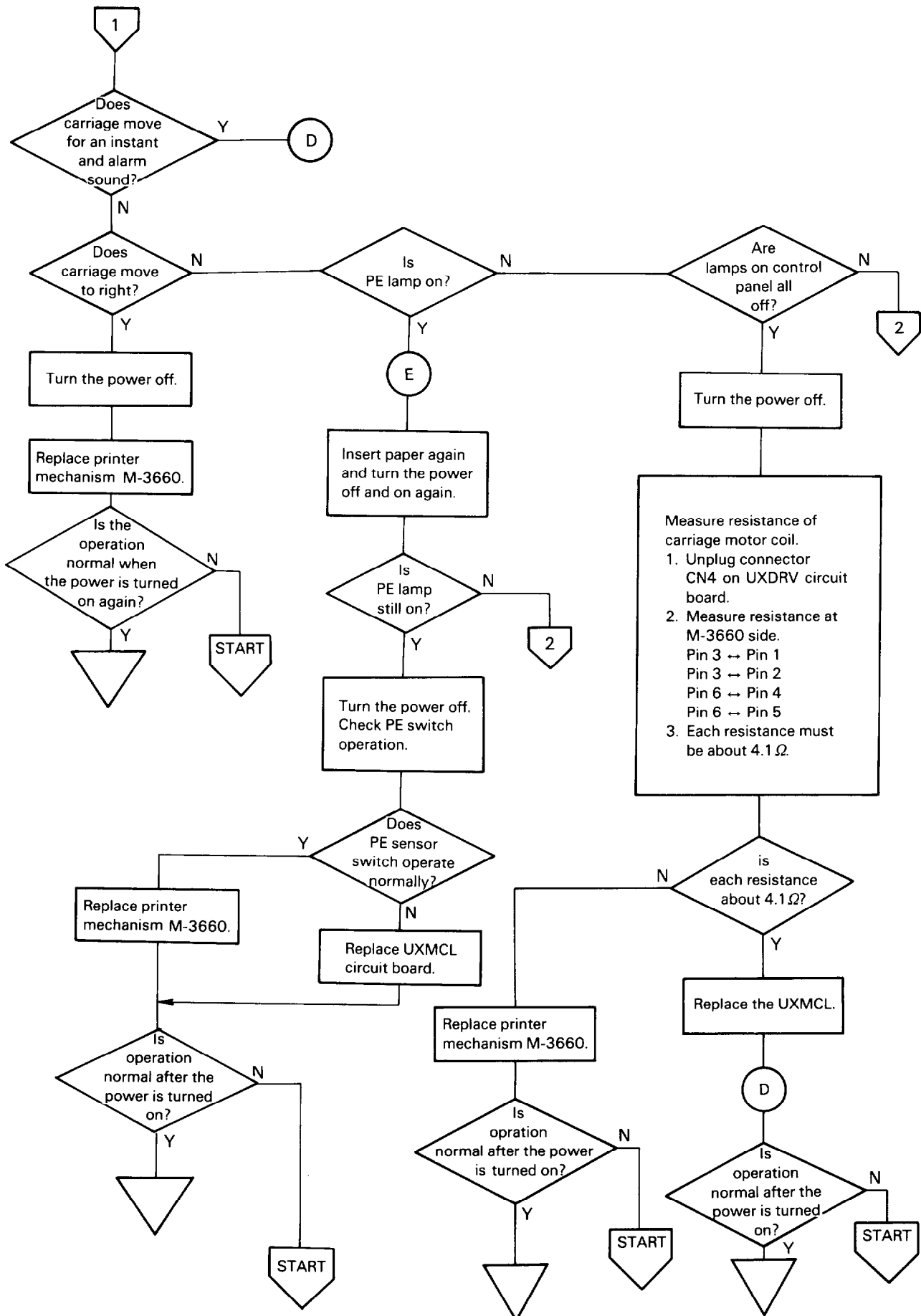




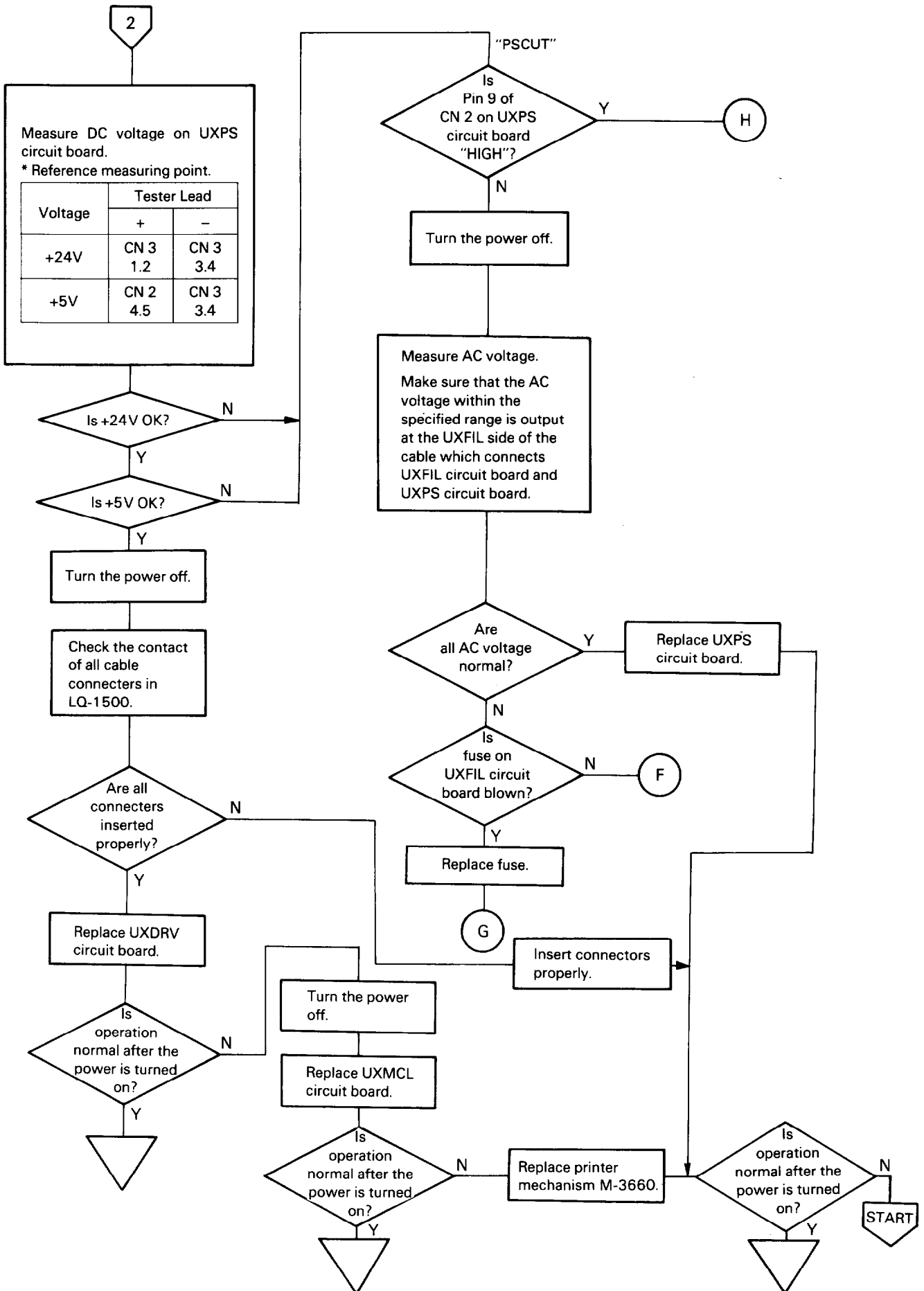


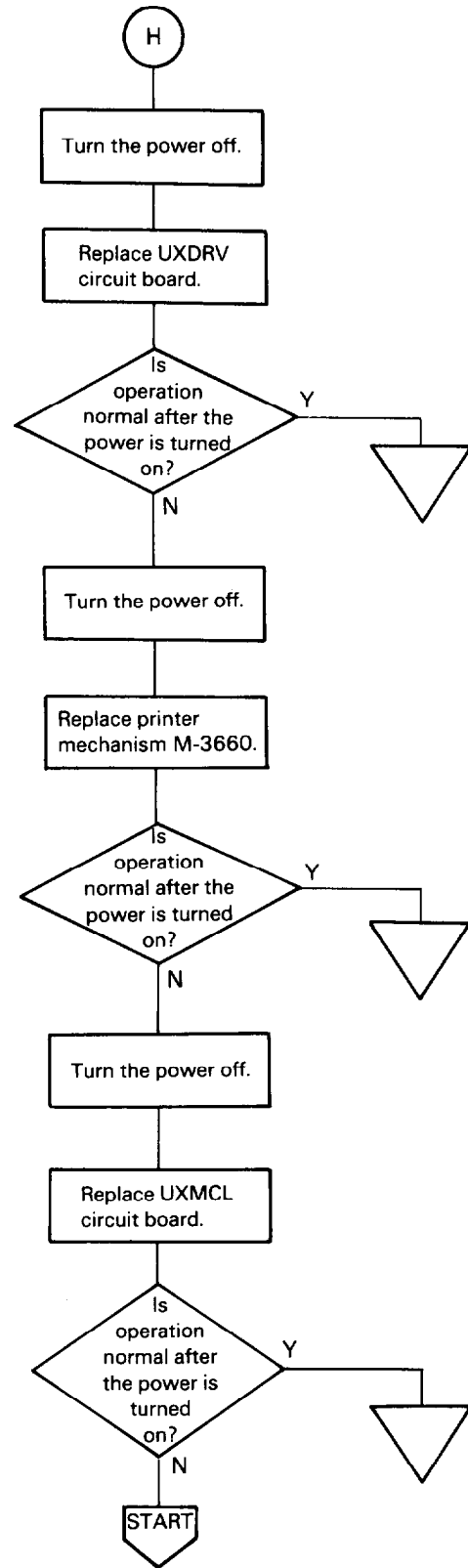
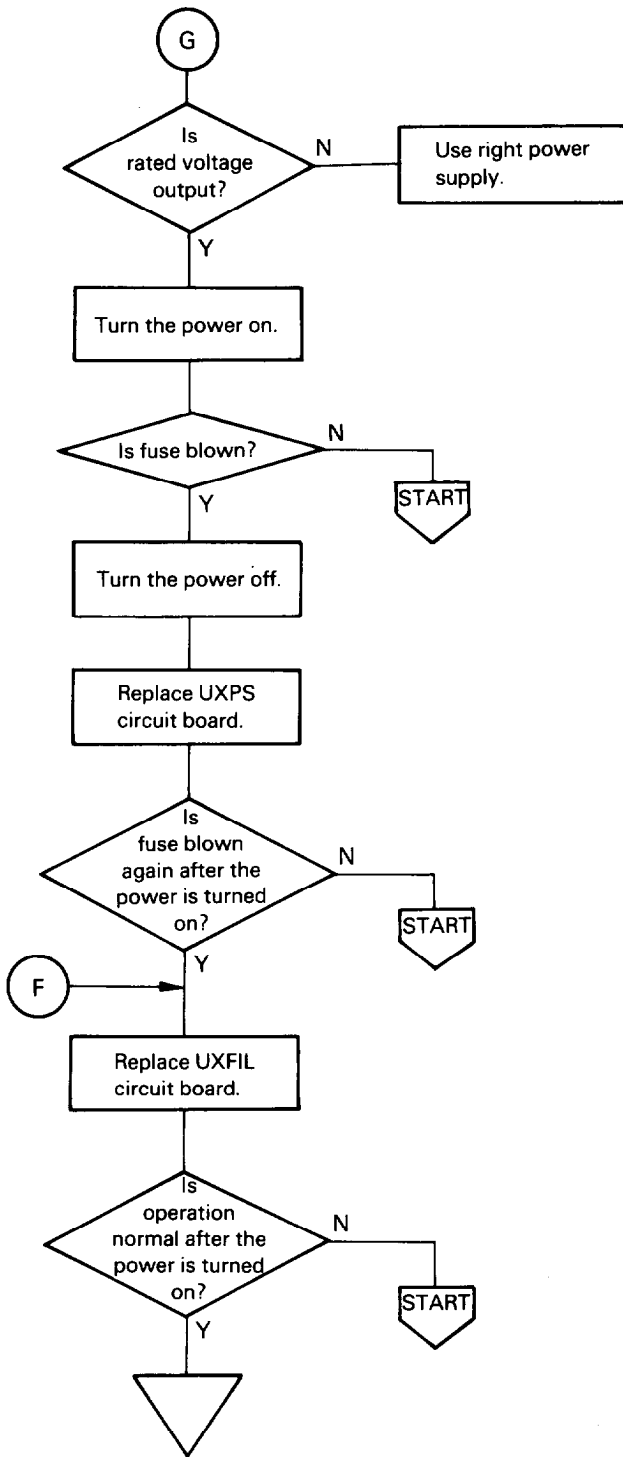


< Carriage does not return to home position when power switch is turned on. >

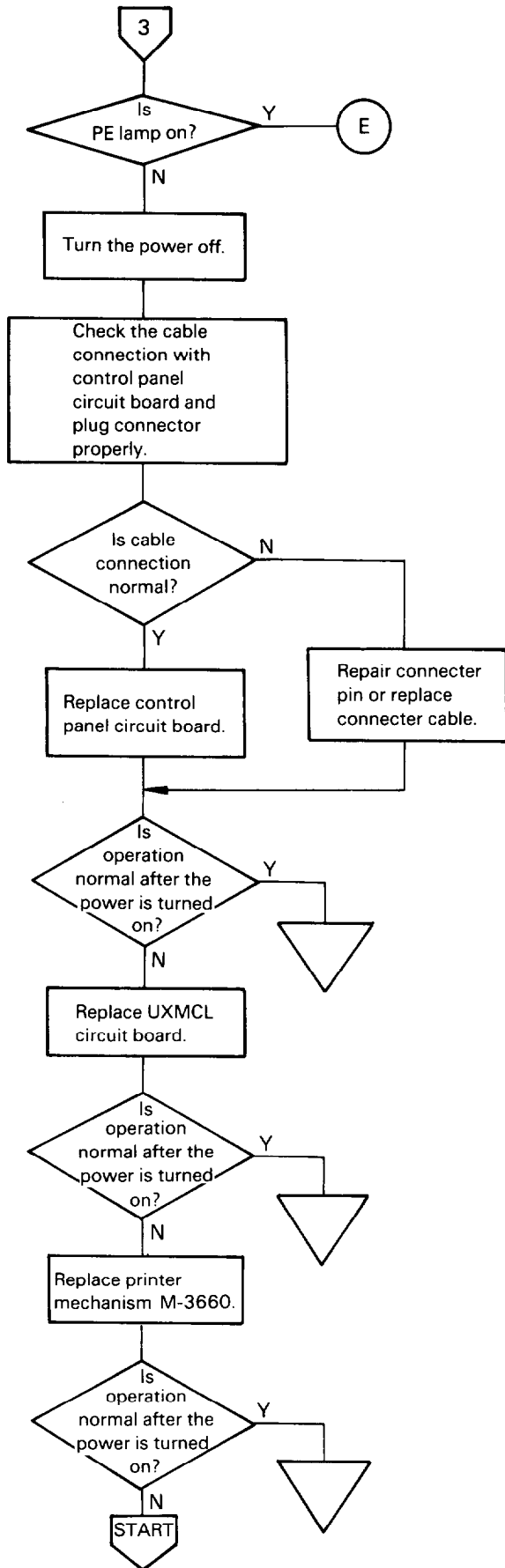


<Carriage does not move. >

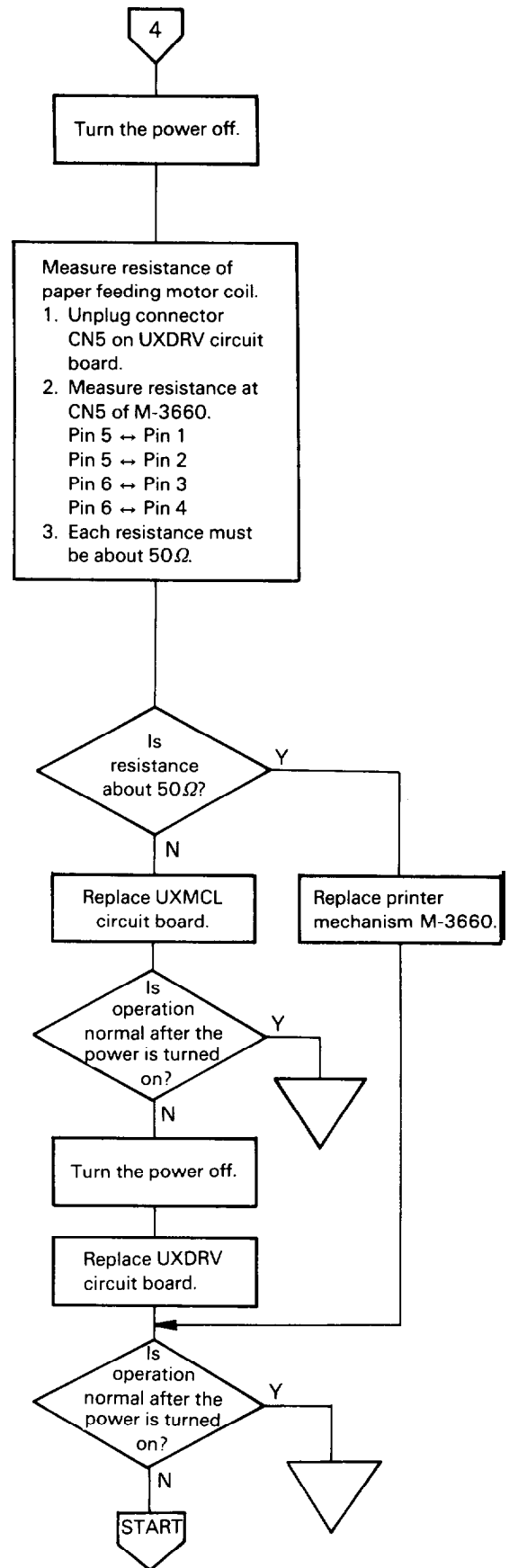




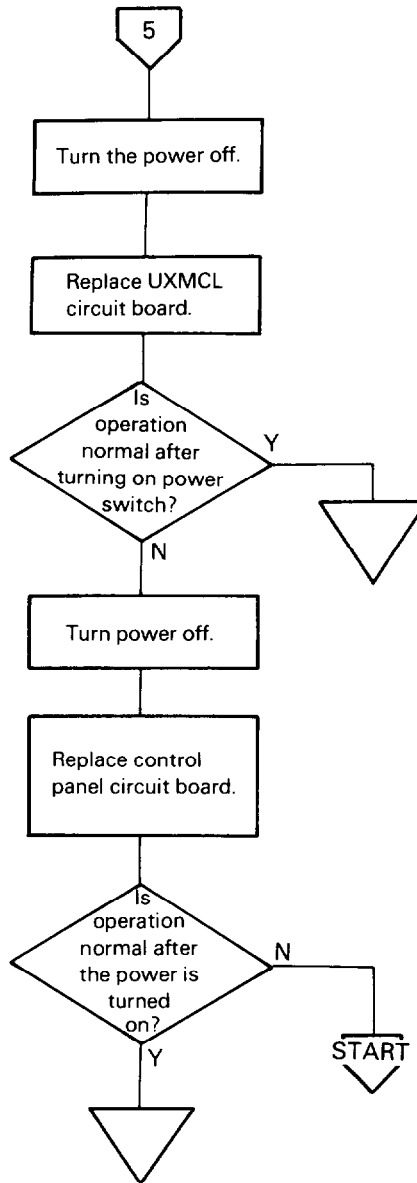
<Control panel indication is faulty. >



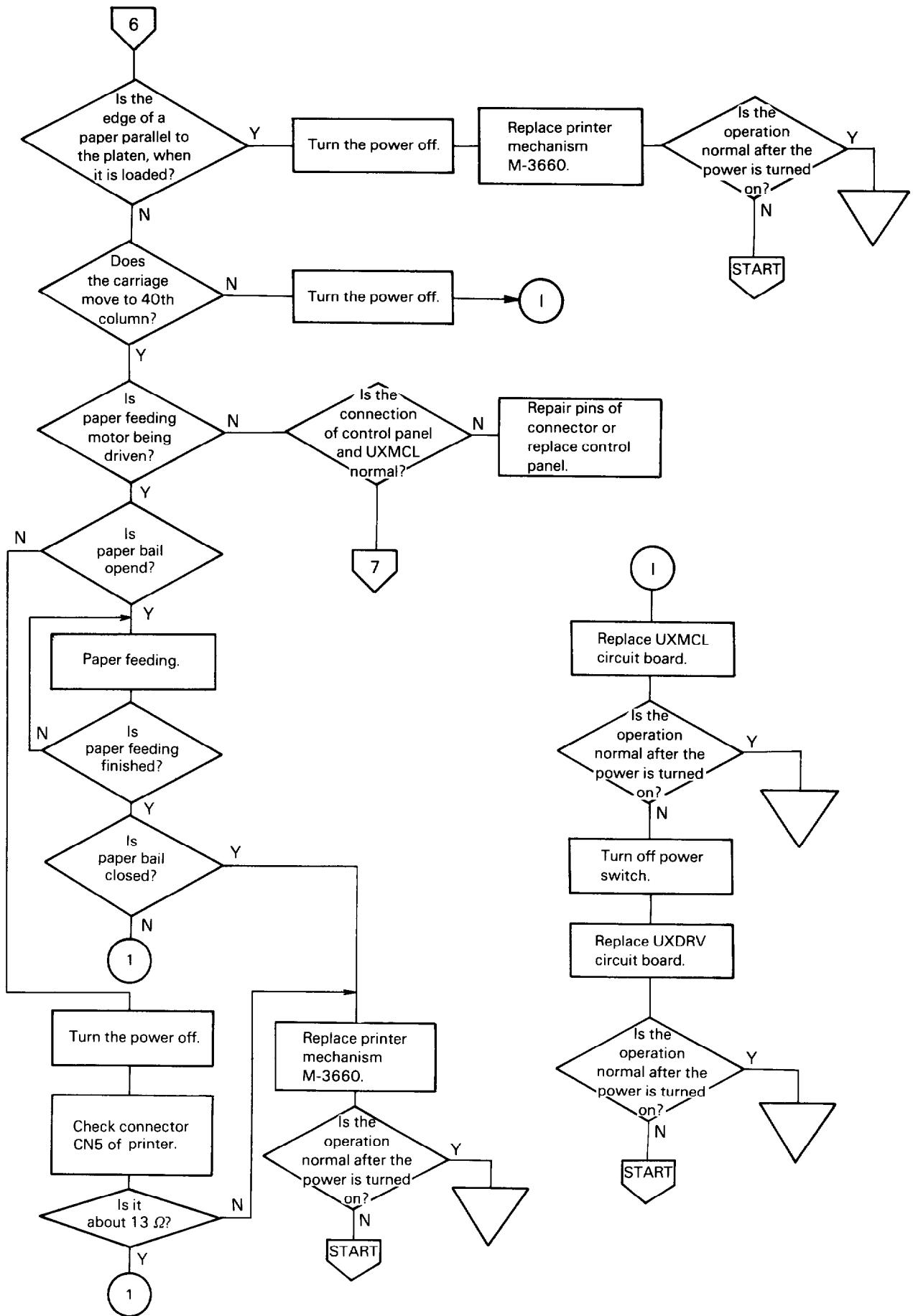
< Paper feeding motor does not stop. >



<Switch on control panel can operate in the on-line state. >

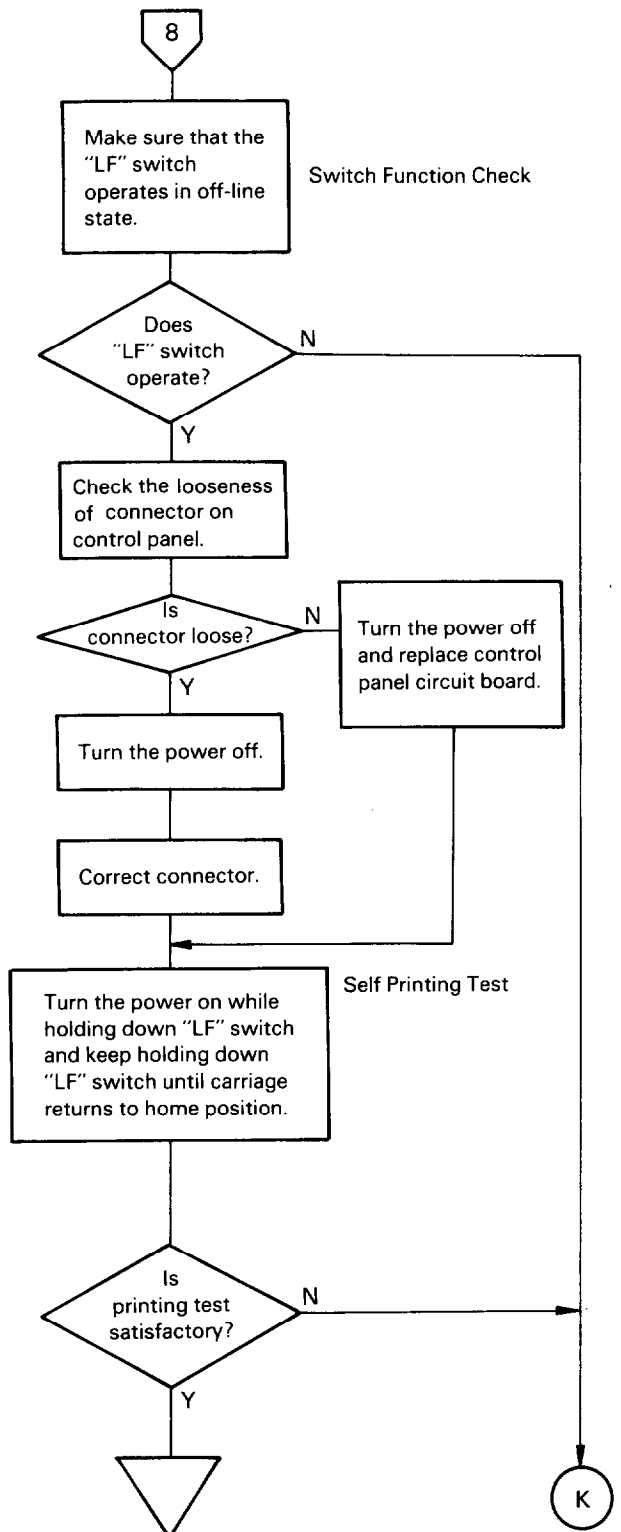
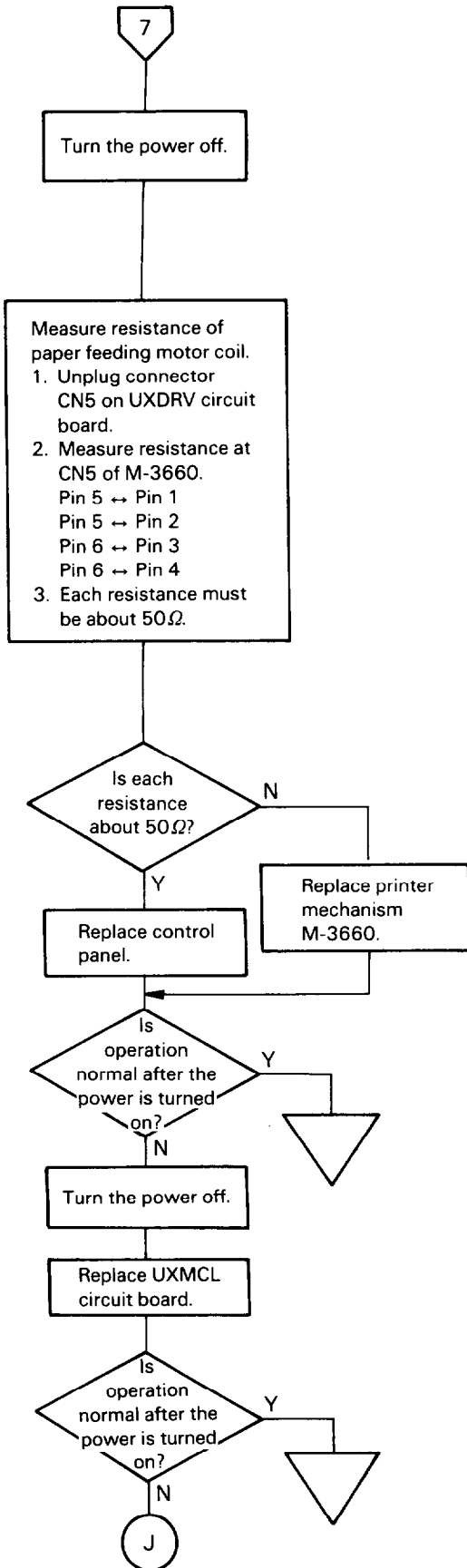


< Sheet loading does not work properly. >

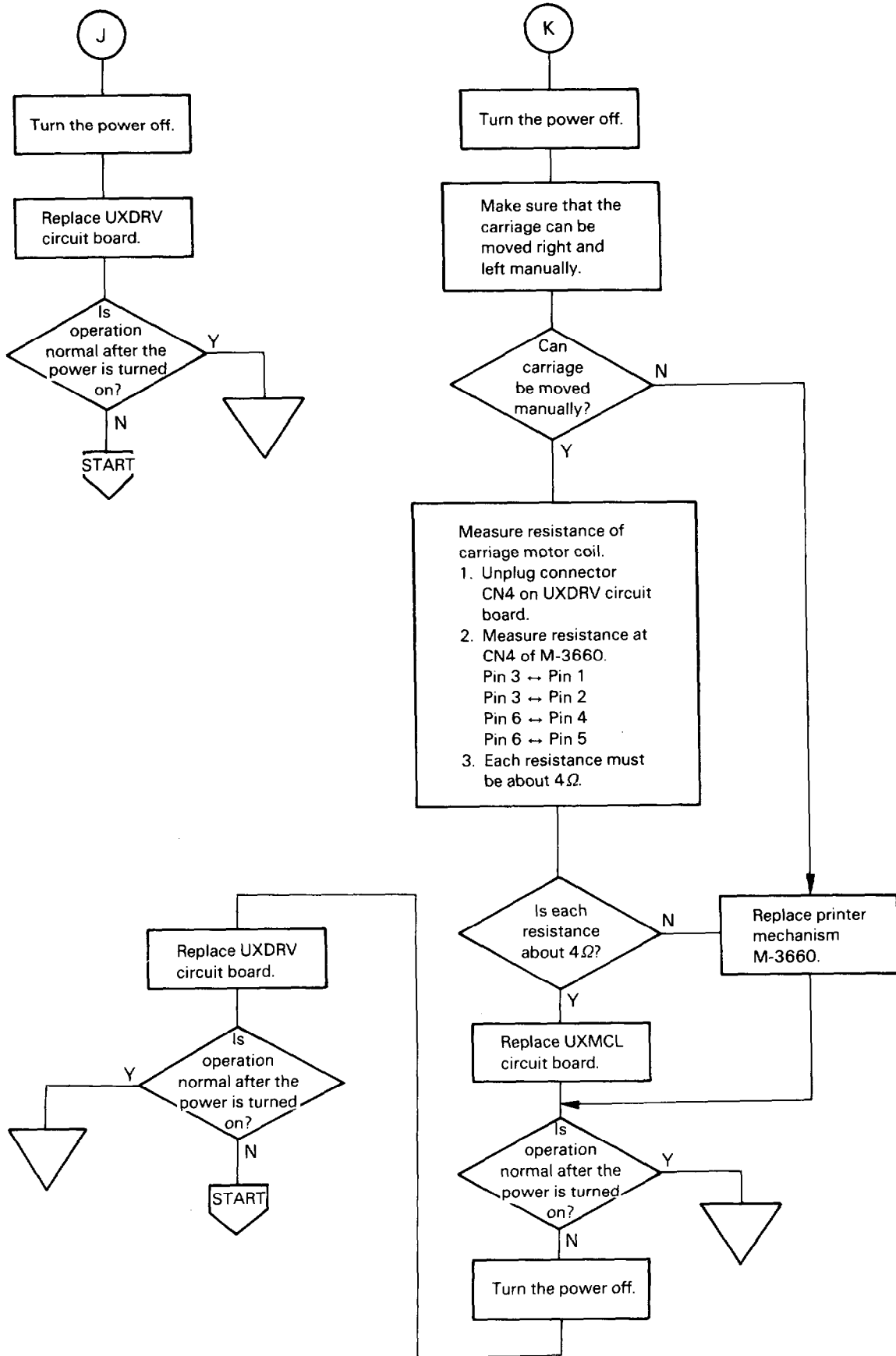


<"LF" and "FF" switches does not operate in off-line state. >

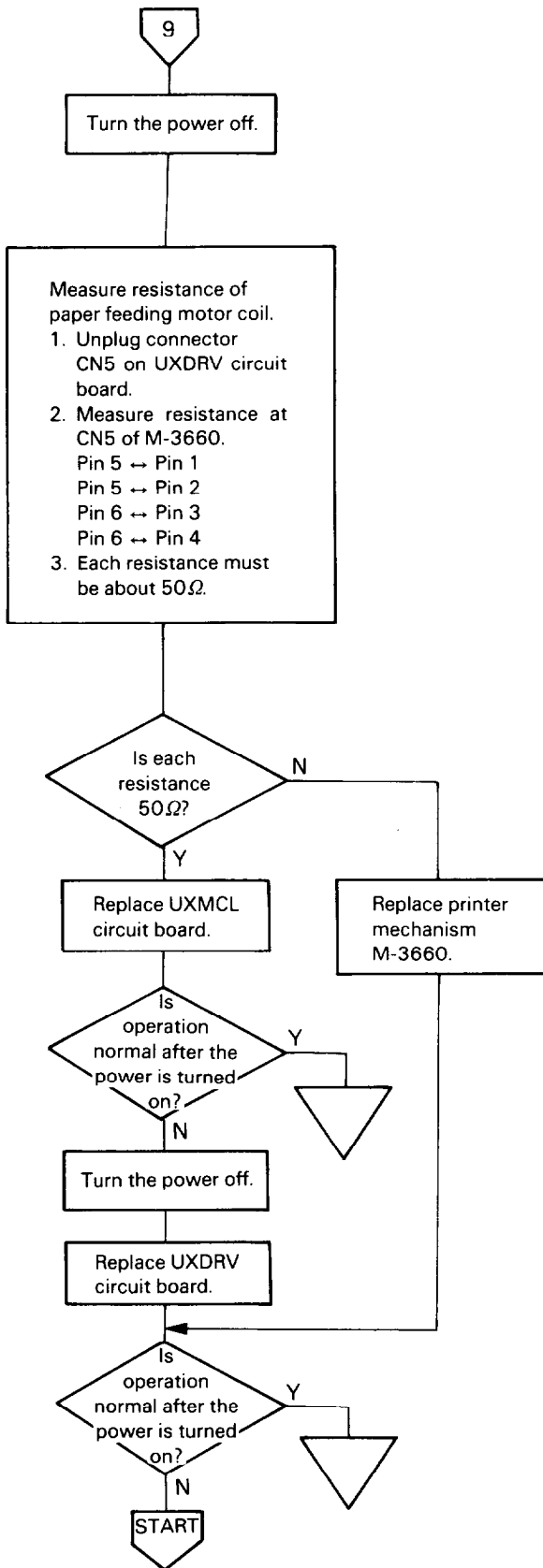
< Carriage does not move in Self Printing Test (1). >



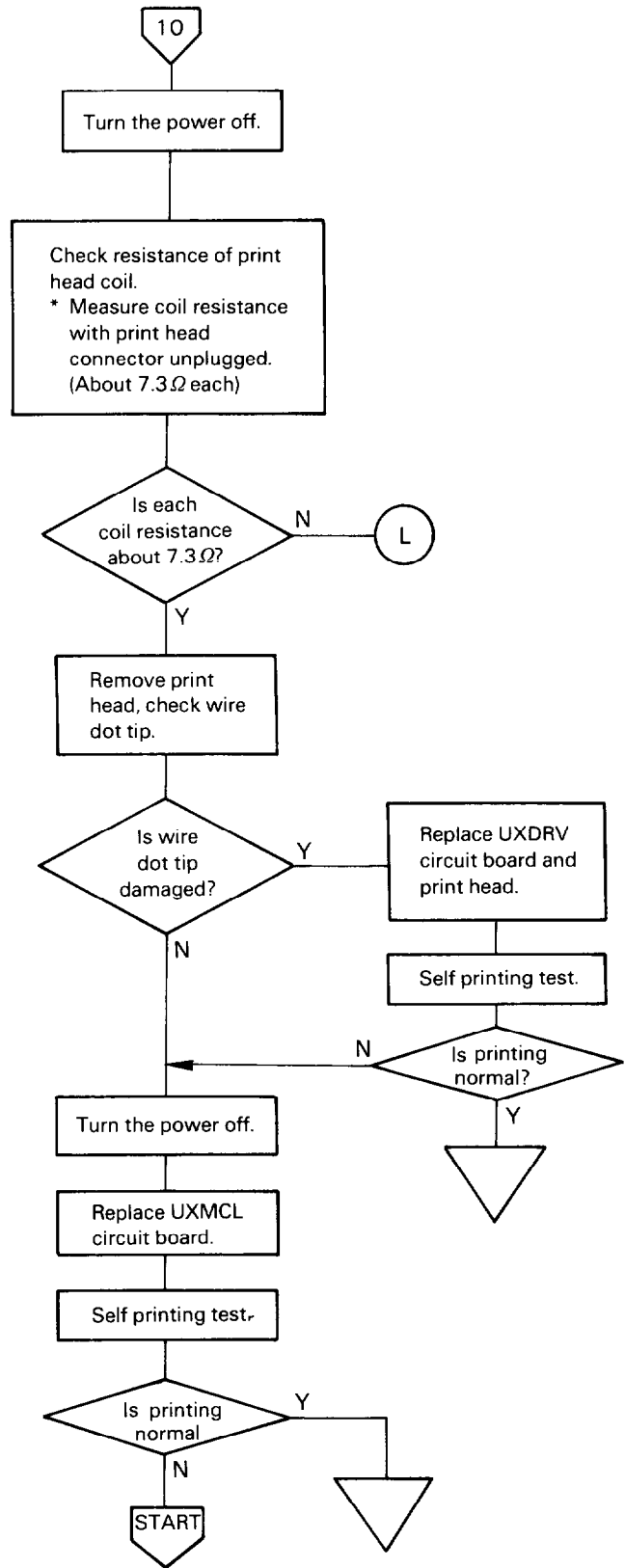
< Carriage does not move in Self-Printing Test (2). >



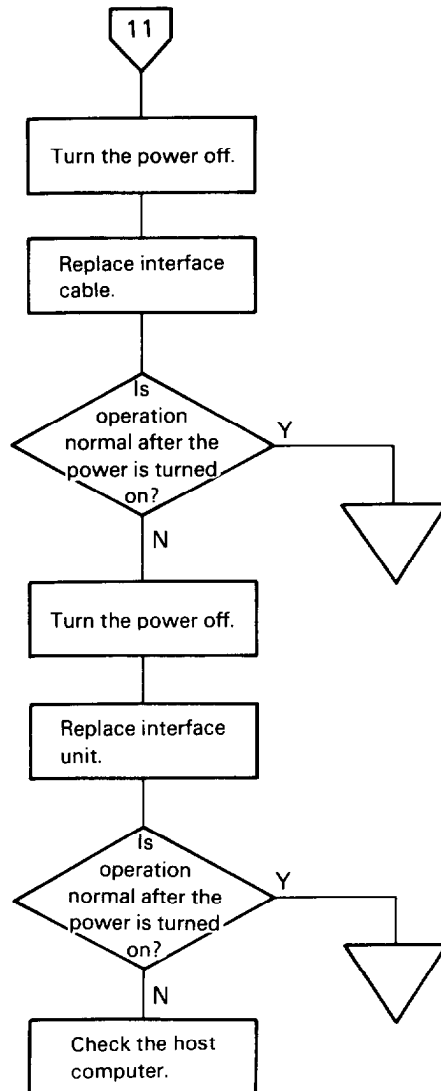
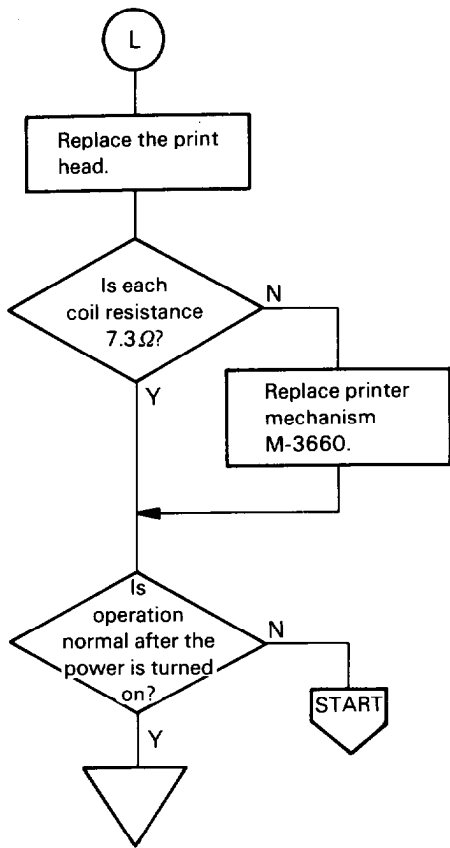
<Paper feeding is not made in Self Printing Test.>



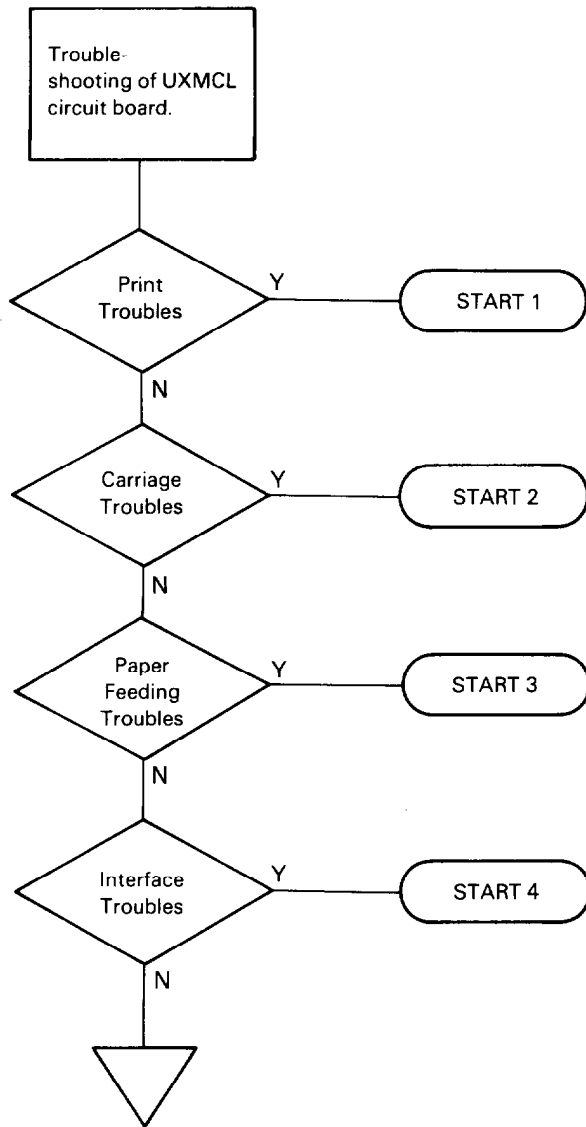
< Printing is faulty. >



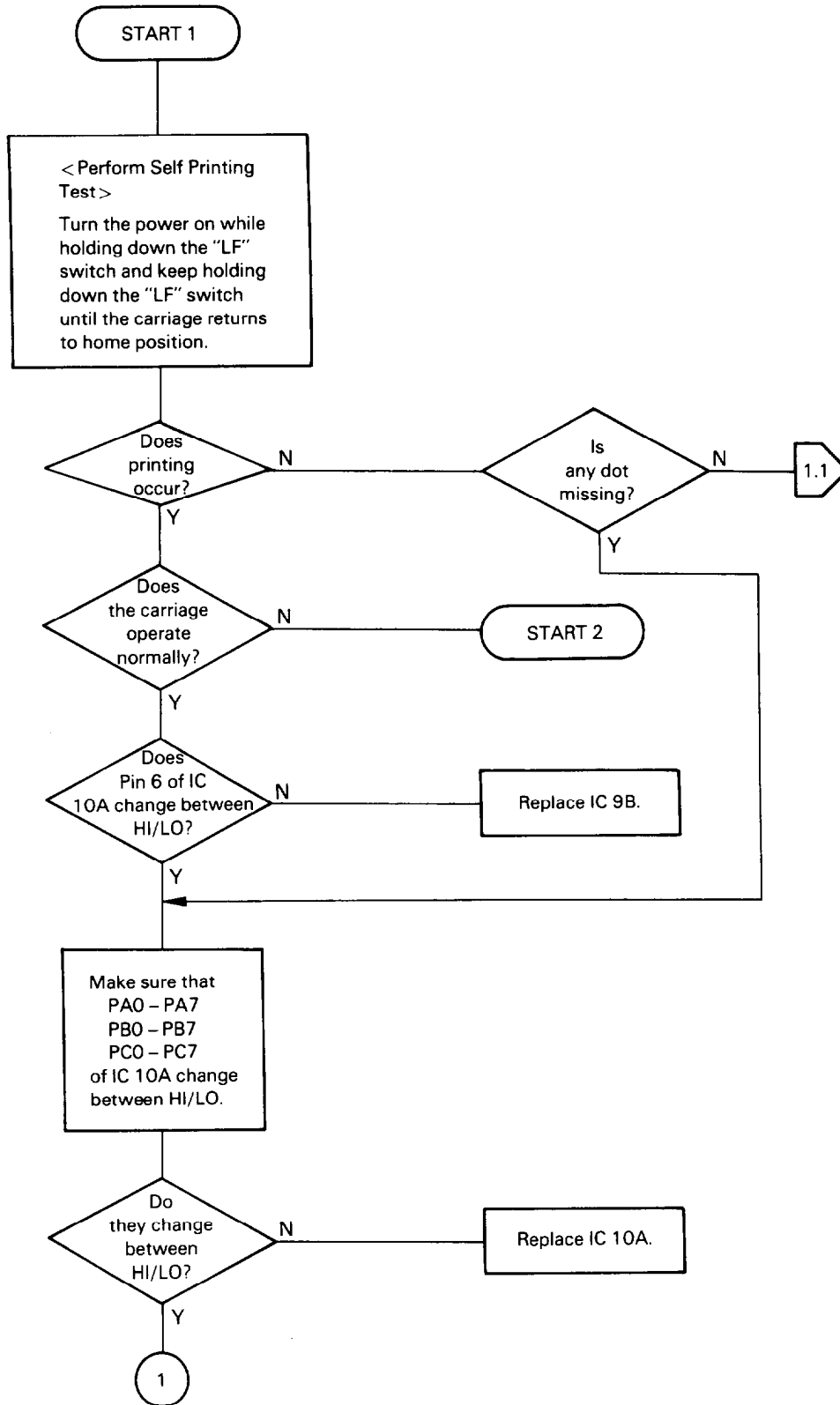
< Operation is abnormal when connected with host computer. >

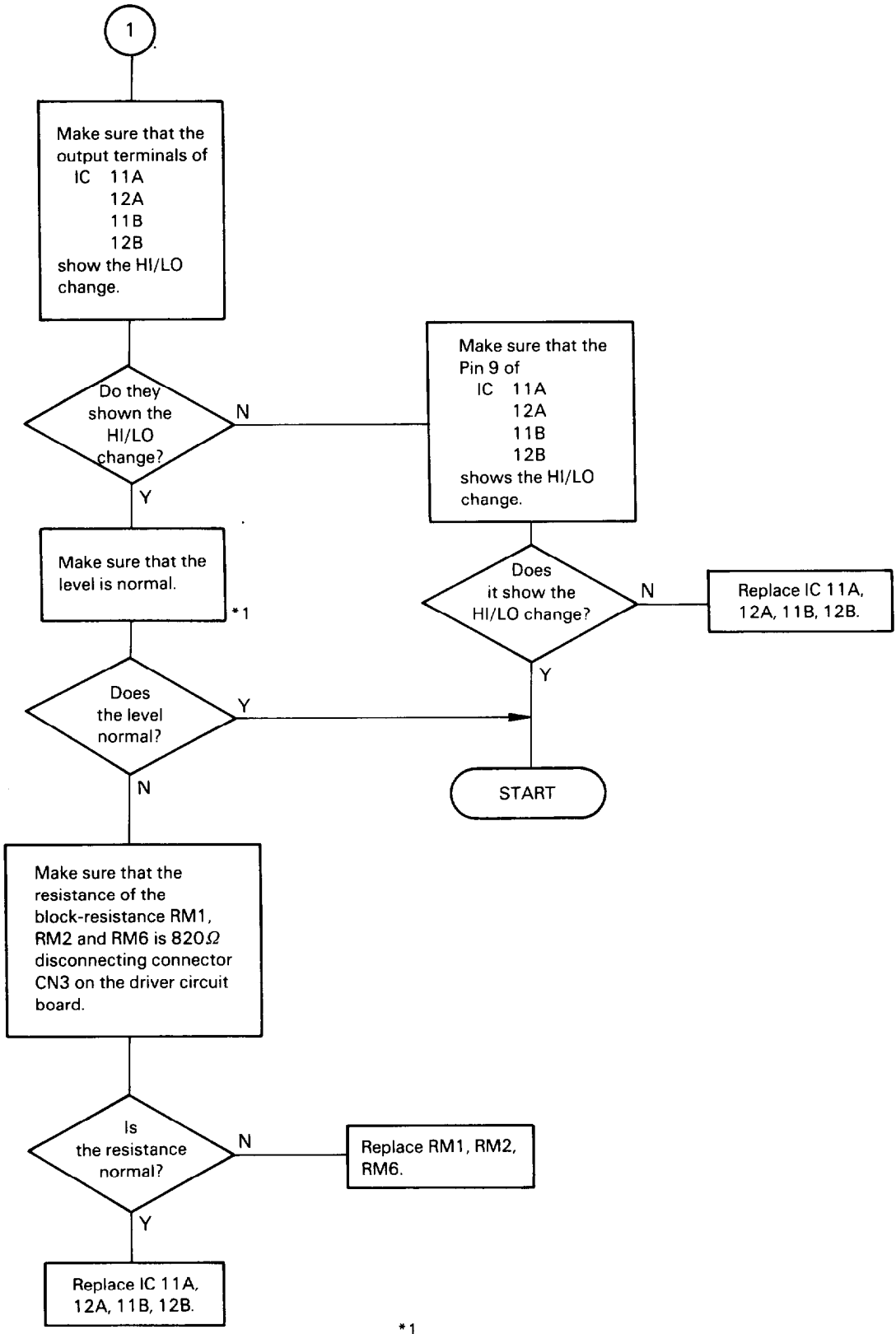


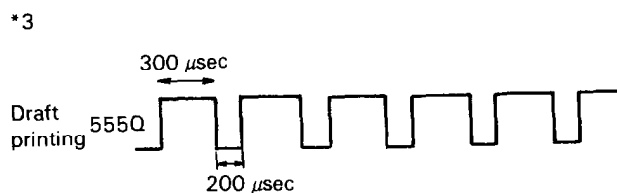
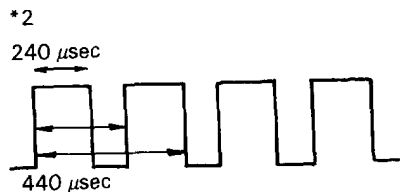
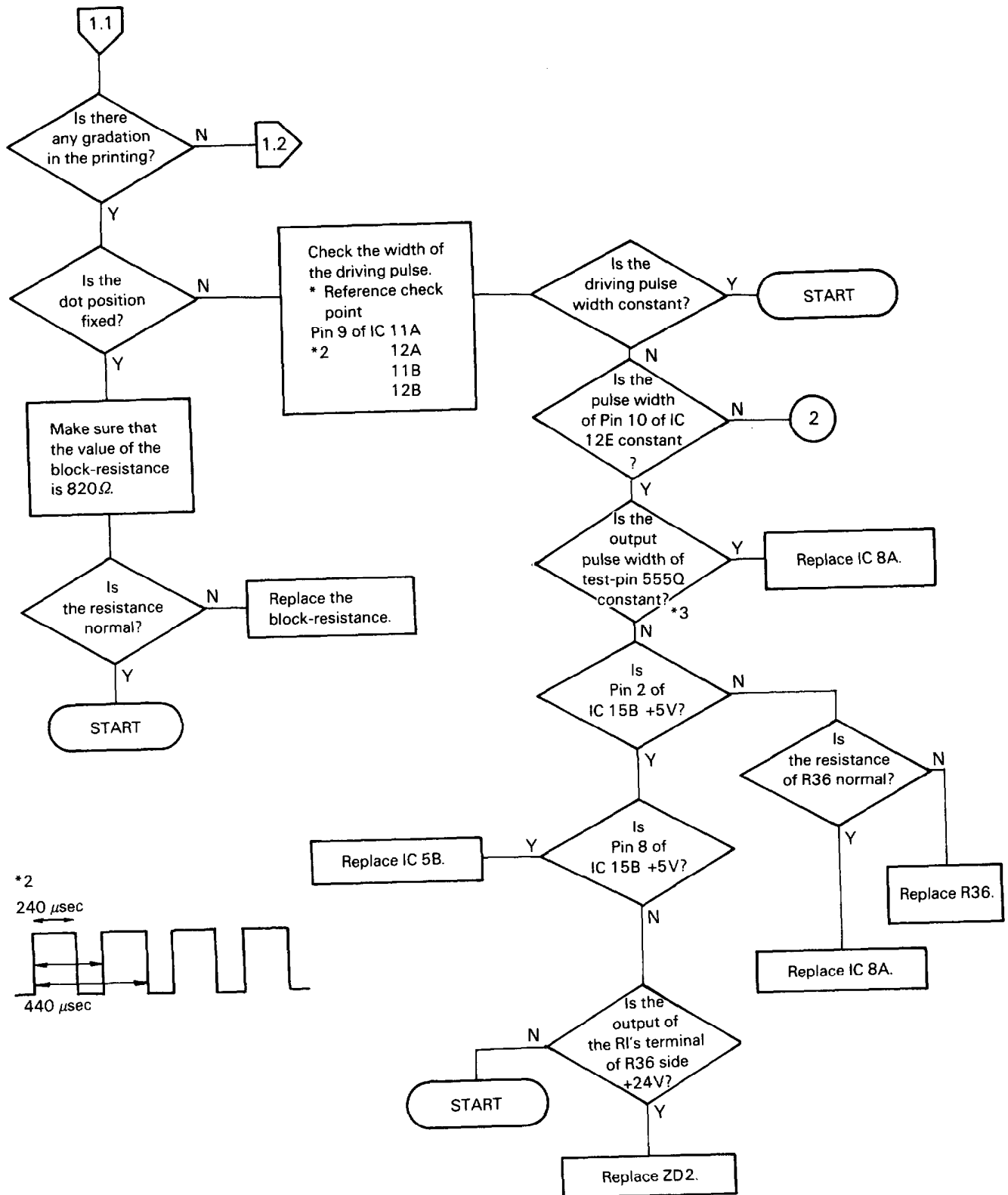
5.3 Unit Repair Flow Chart (UXMCL)

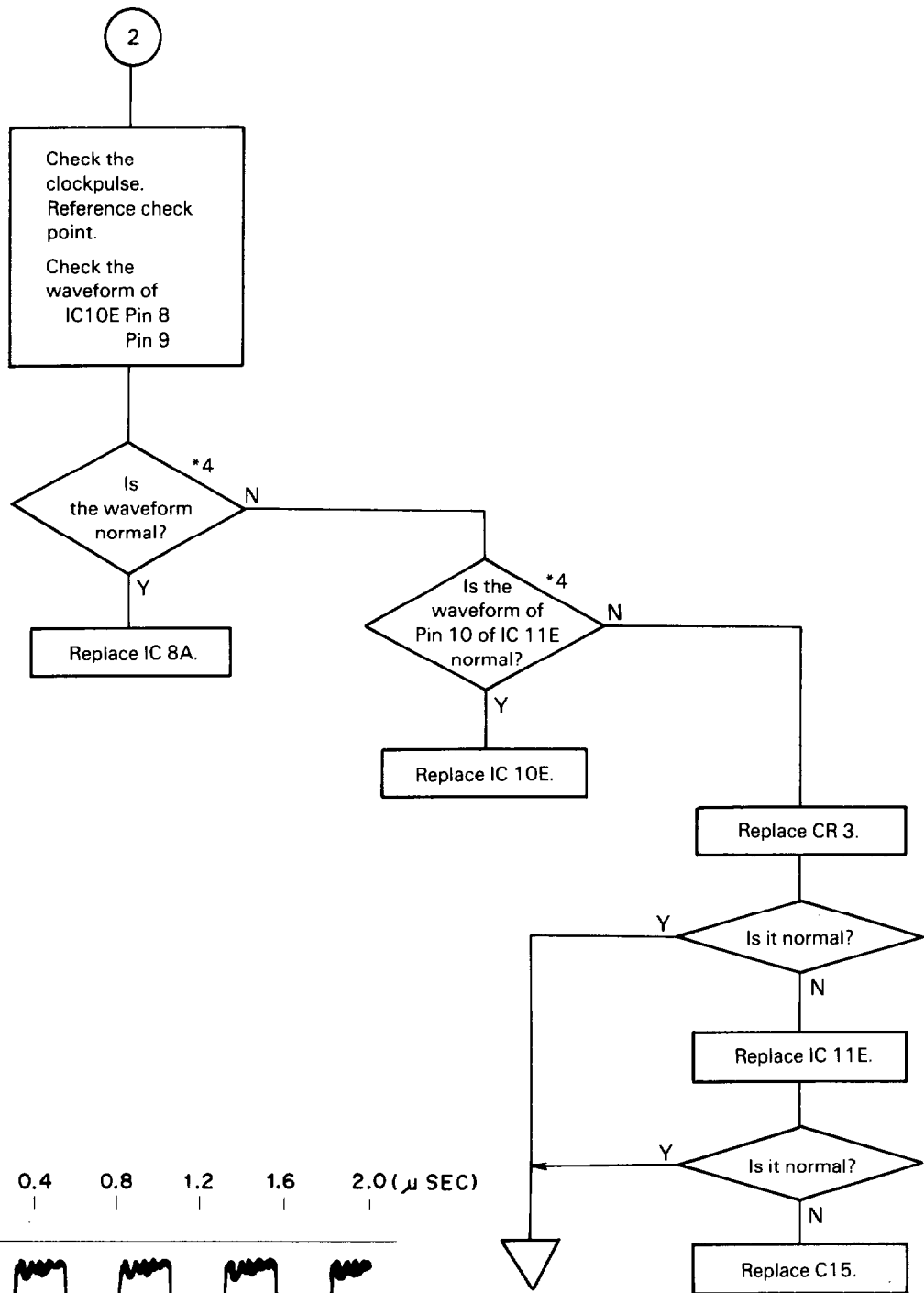


1. Printing Troubles

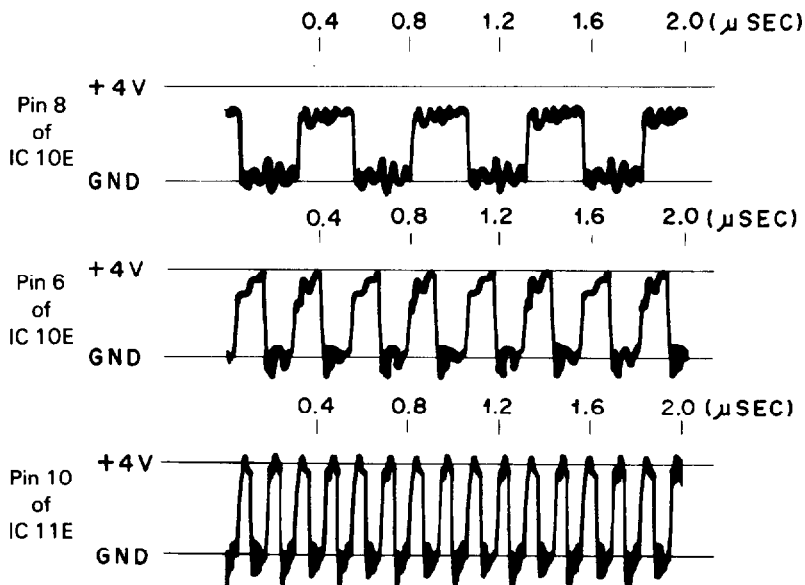


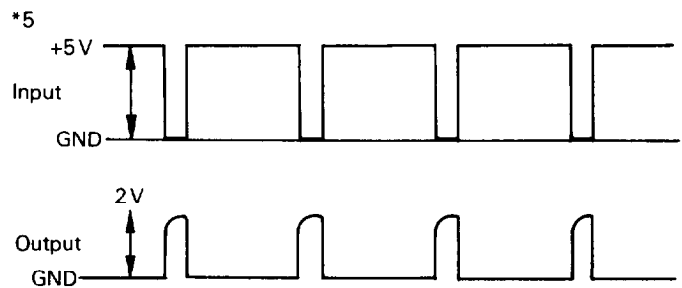
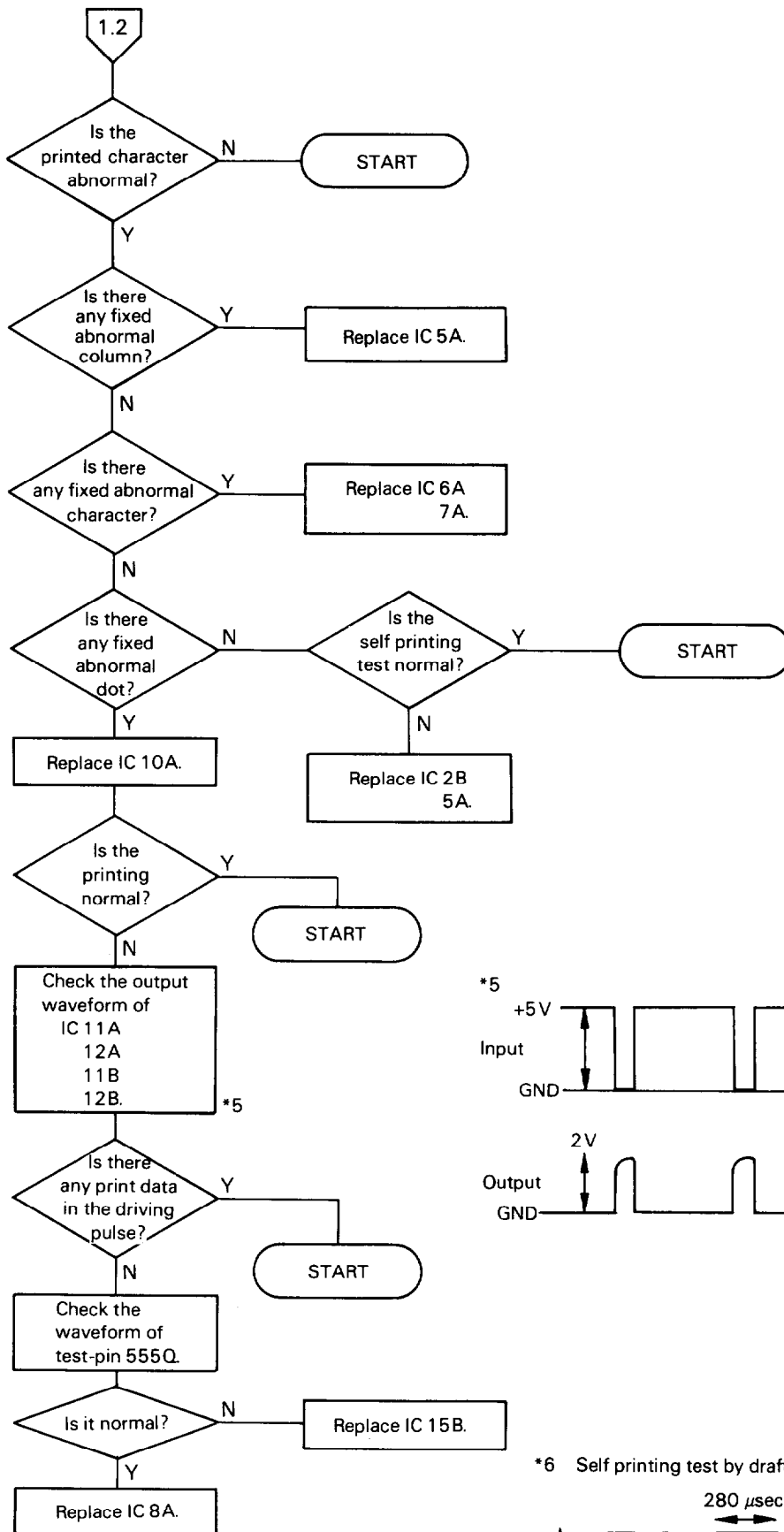




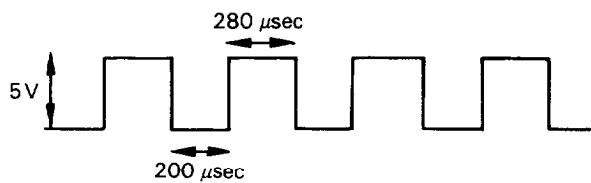


*4 Reference waveform

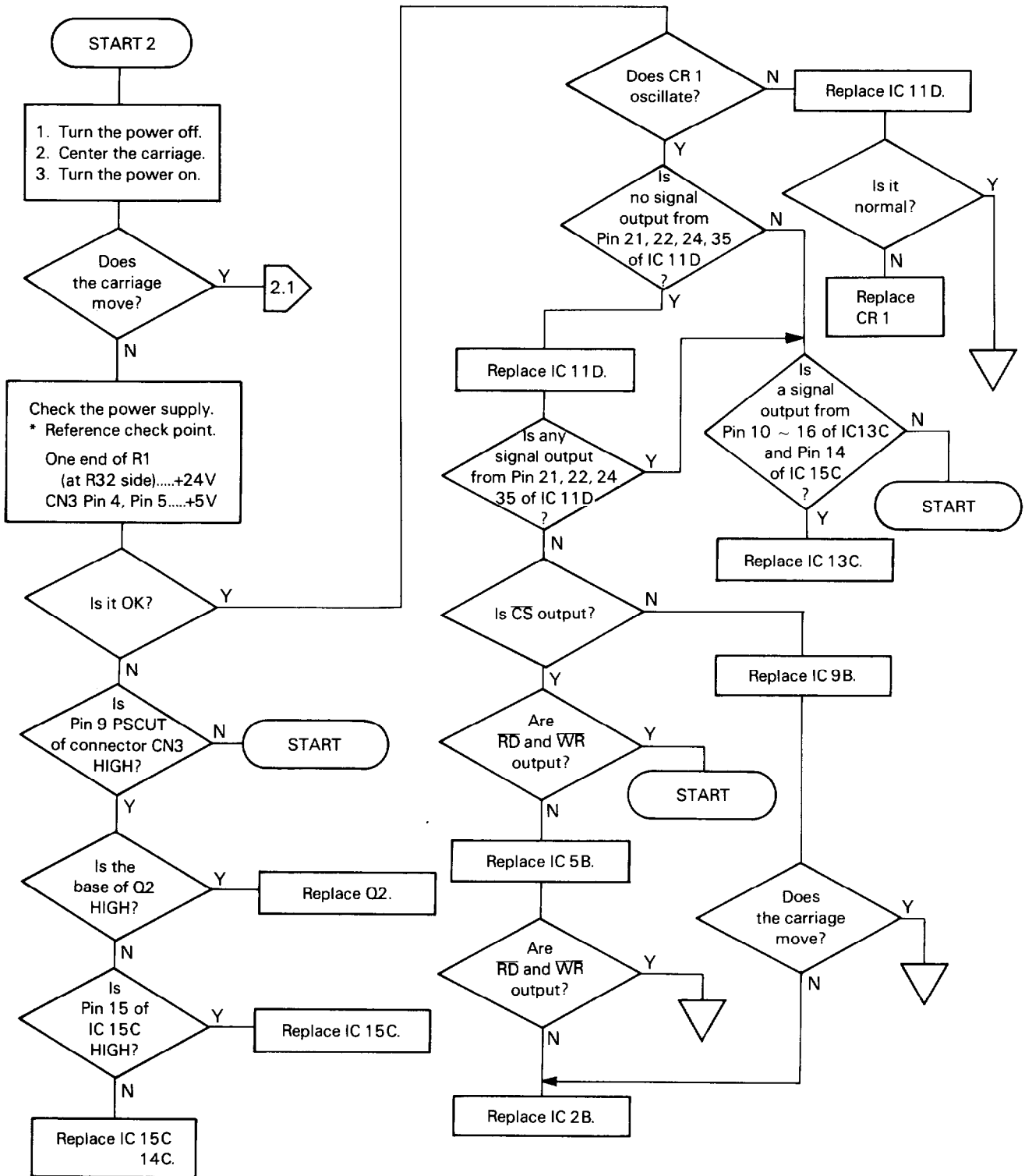


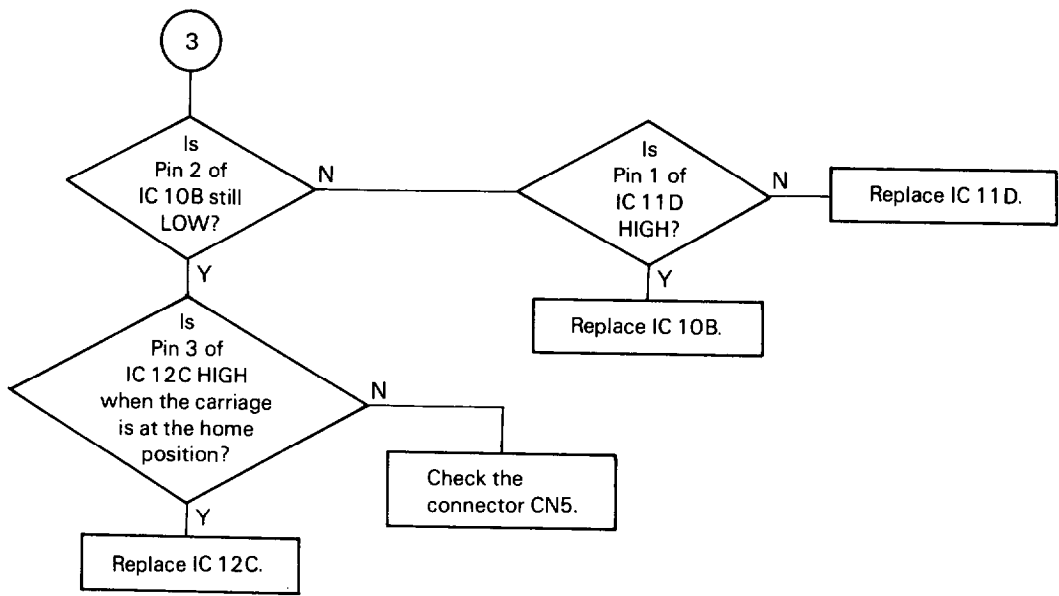
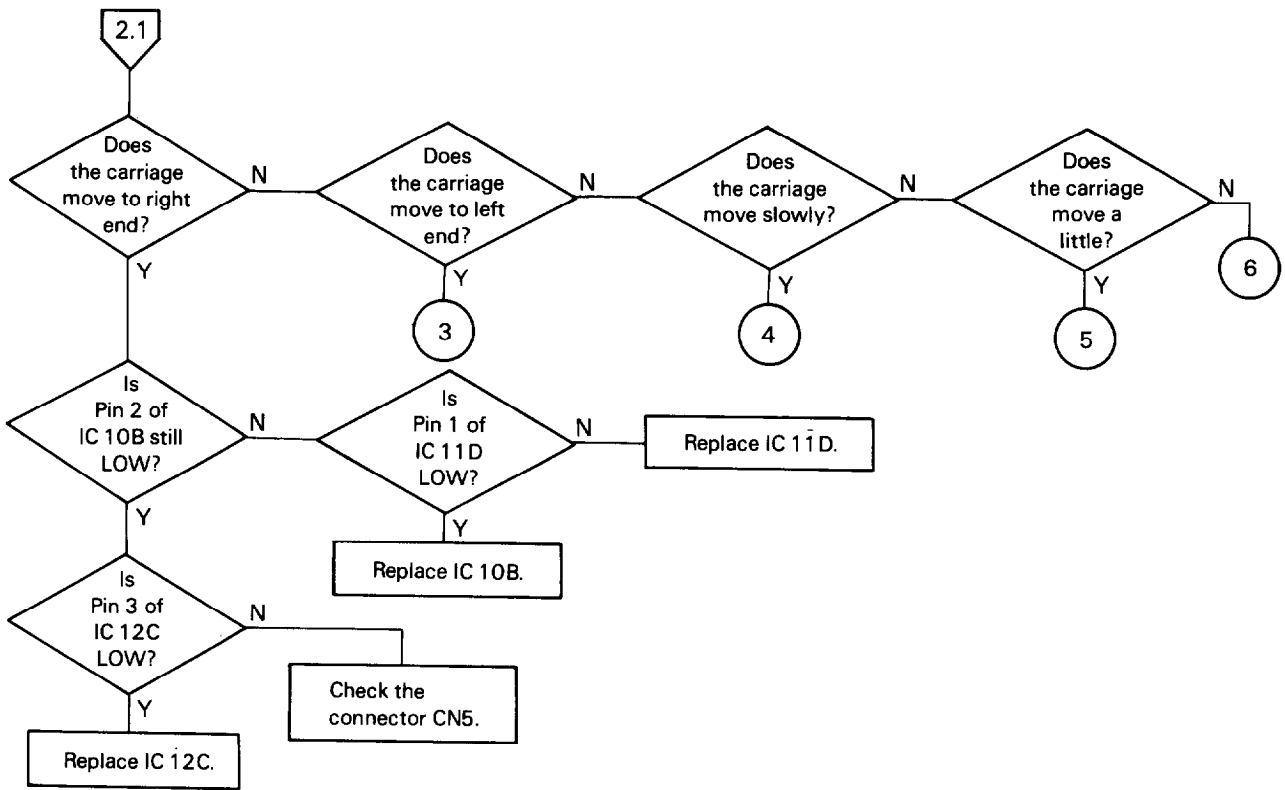


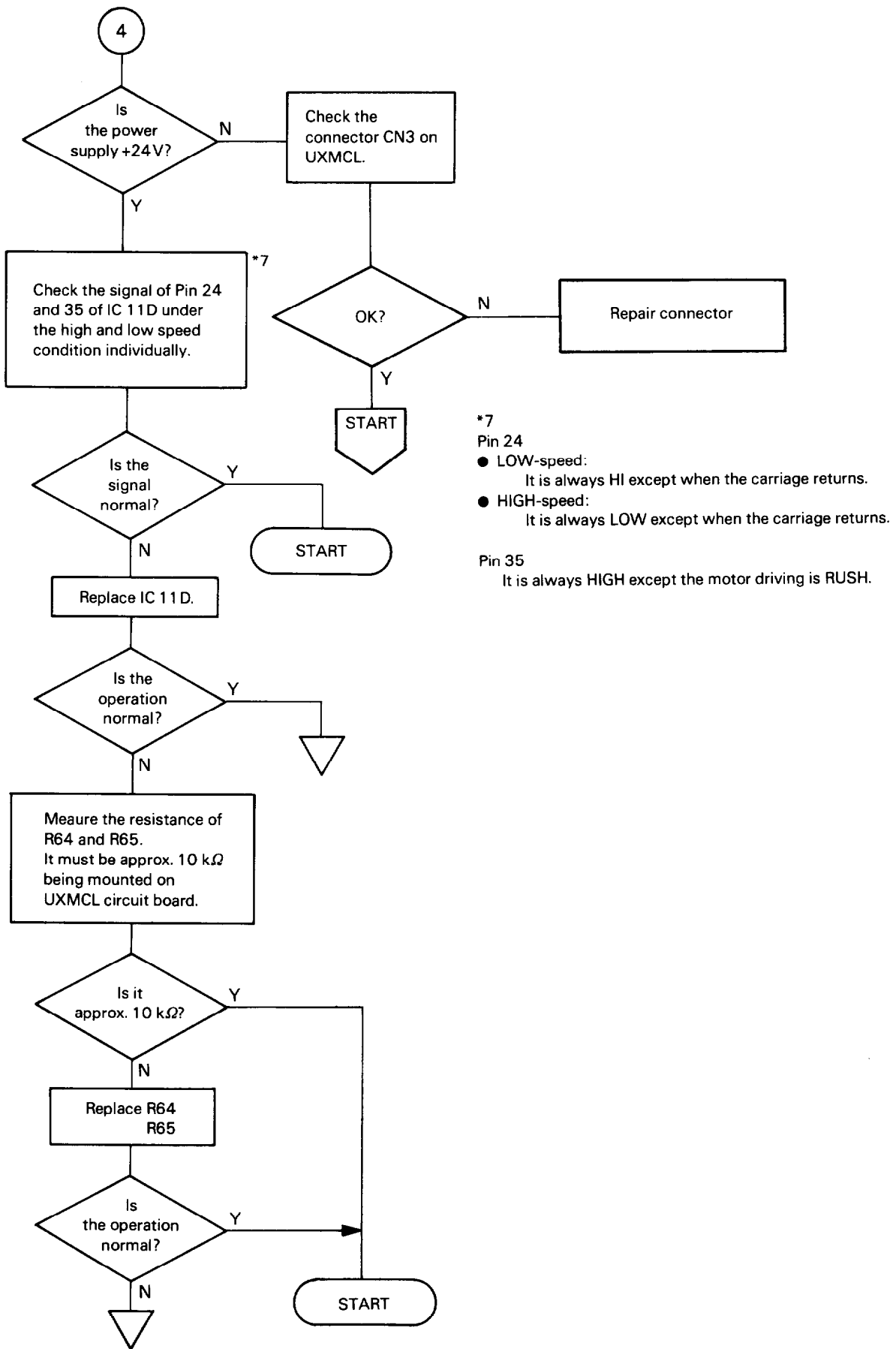
*6 Self printing test by draft mode

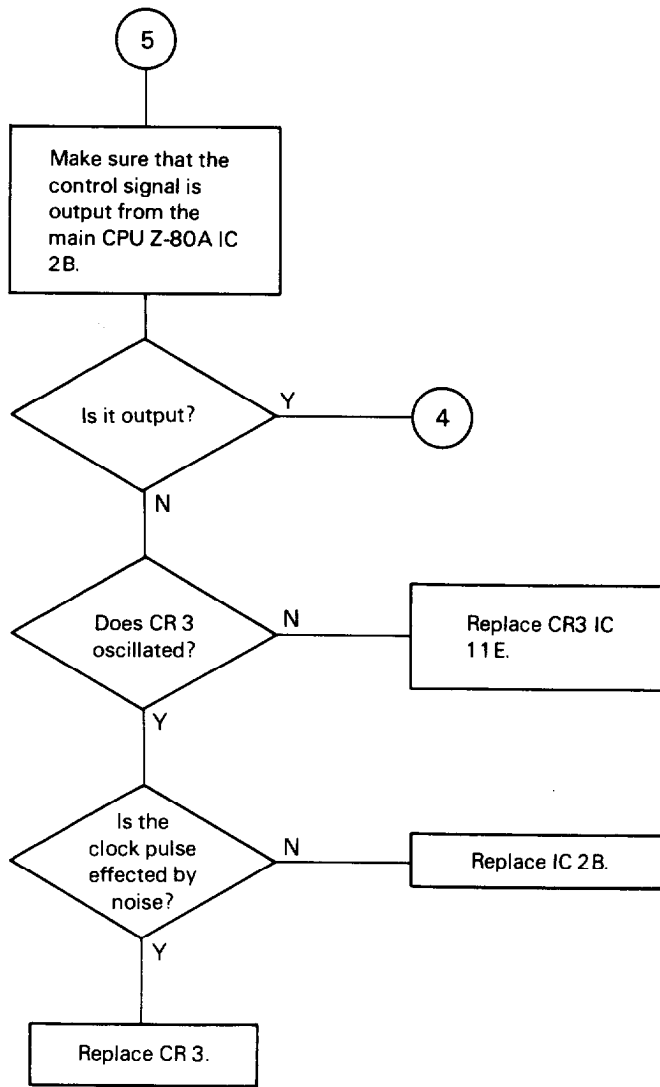


2. Carriage Troubles









6

Make sure that when the carriage operates, there is no abnormal sound and STK 6982 on the driver circuit board is not over-heated.

Is the output waveform of STK 6982 normal? ^{*8}

START

Measure the resistance of R42 and R43 on the UXMCL board. It must be approx. 8.2 kΩ.

Is it approx. 8.2 kΩ?

The resistance must be 8.2 kΩ when one of pins is cut, otherwise, replace the resistance.

Measure the resistance of R71, R72 on the UXMCL board. It must be approx. 8.2 kΩ.

Is it approx. 8.2 kΩ?

The resistance must be 15 kΩ when one of pins is cut, otherwise, replace the resistance.

Measure the resistance of R44, R45 on the UXMCL board. It must be approx. 20 kΩ.

Is it approx. 20 kΩ?

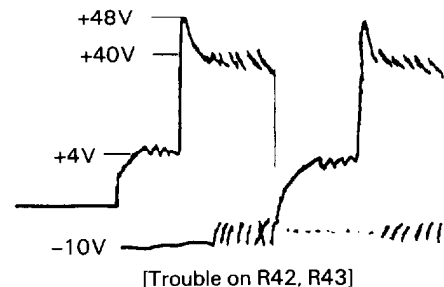
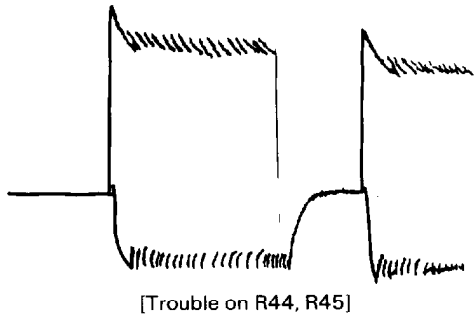
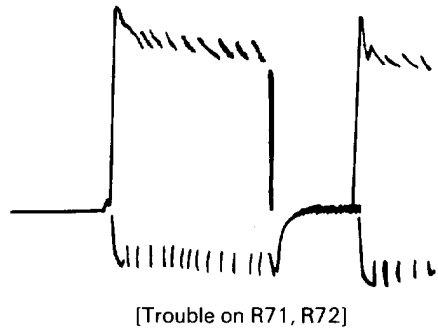
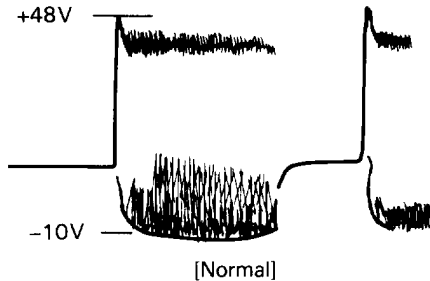
The resistance must be 33 kΩ when one of pins is cut, otherwise, replace the resistance.

START

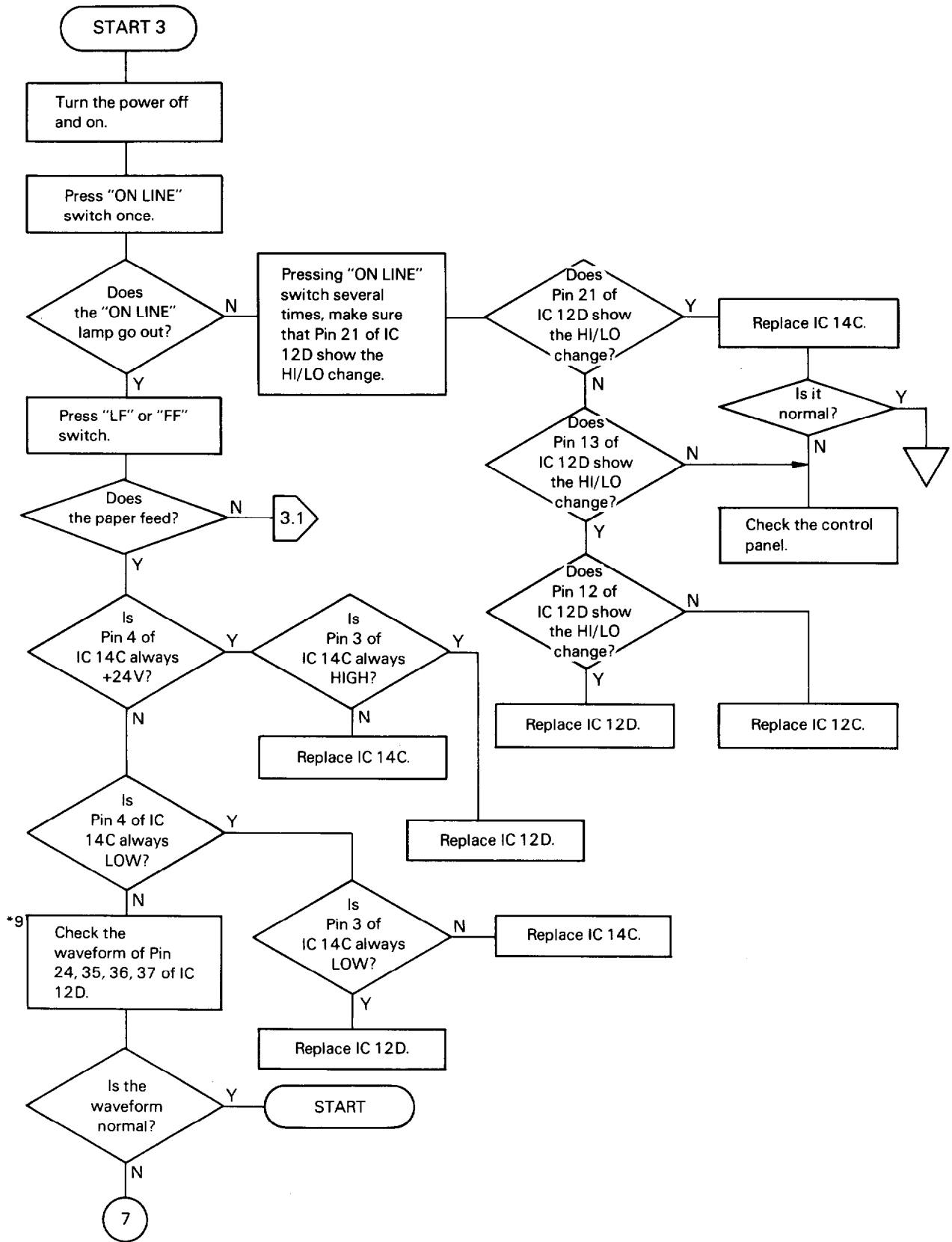
*8

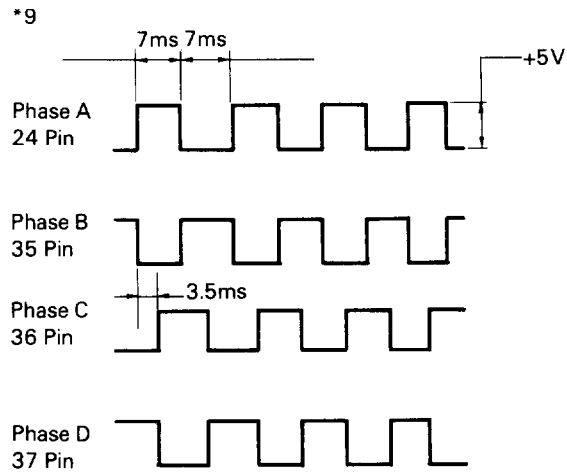
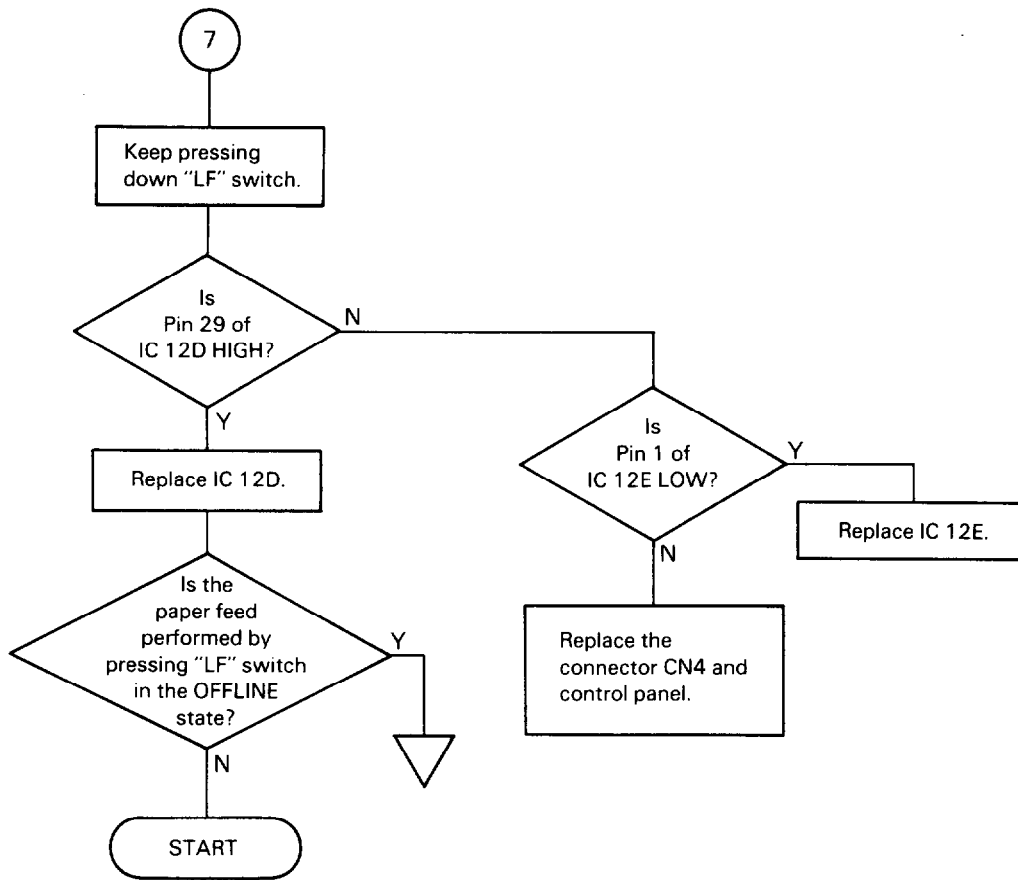
< Output waveform of STK 6982 >

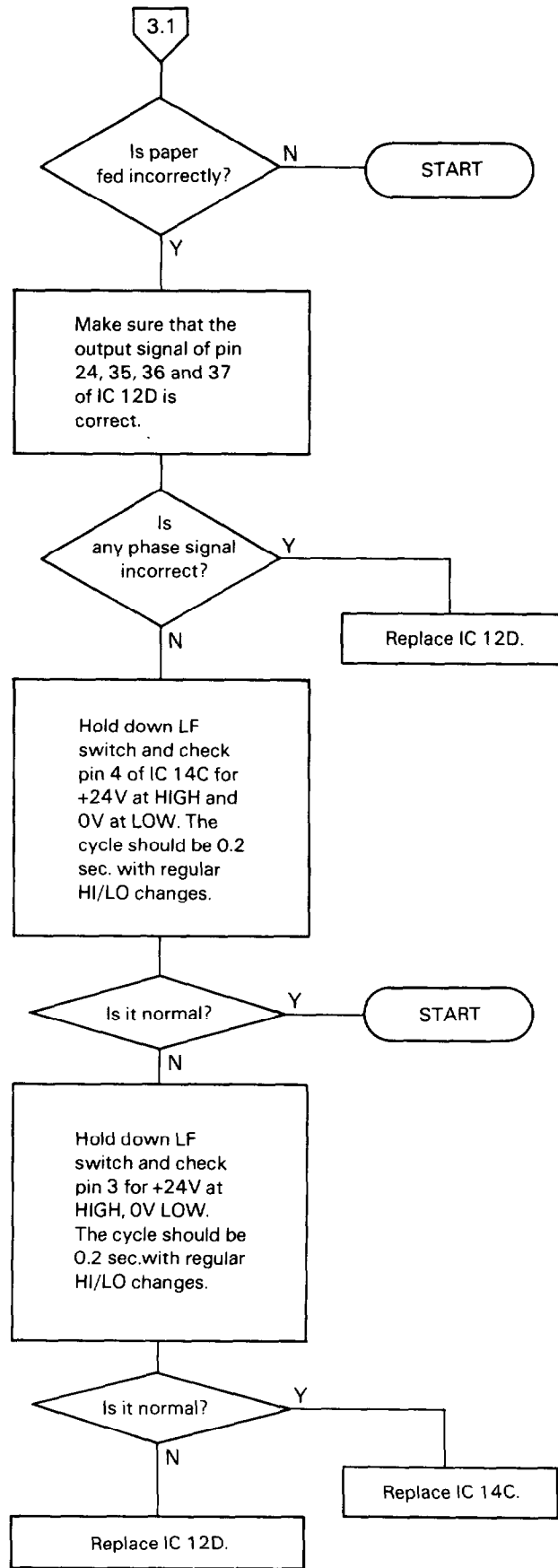
Reference check point; pin 1, 2, 4, 5 of CN4 on UXDRV board.



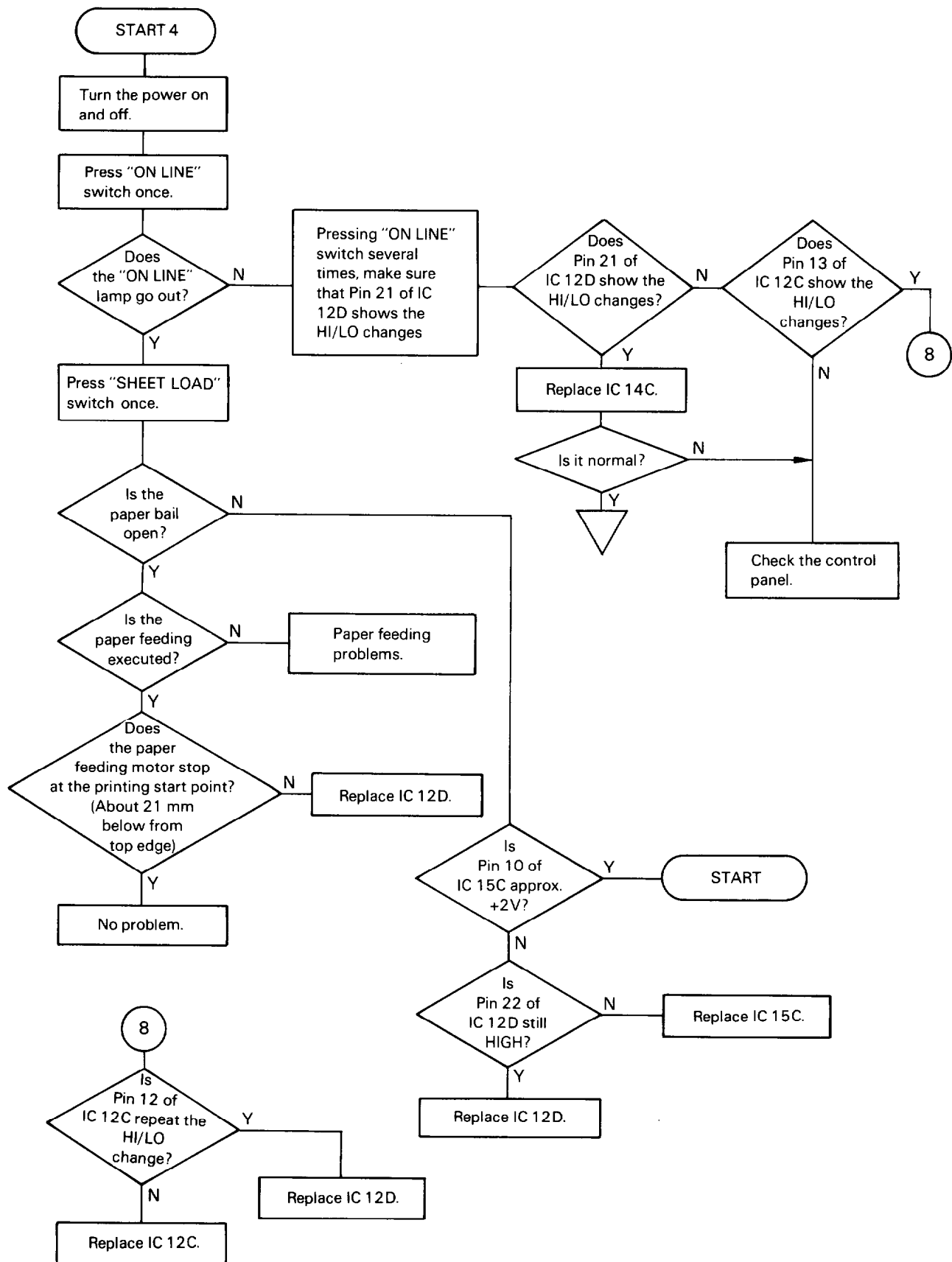
3. Paper Feeding Troubles



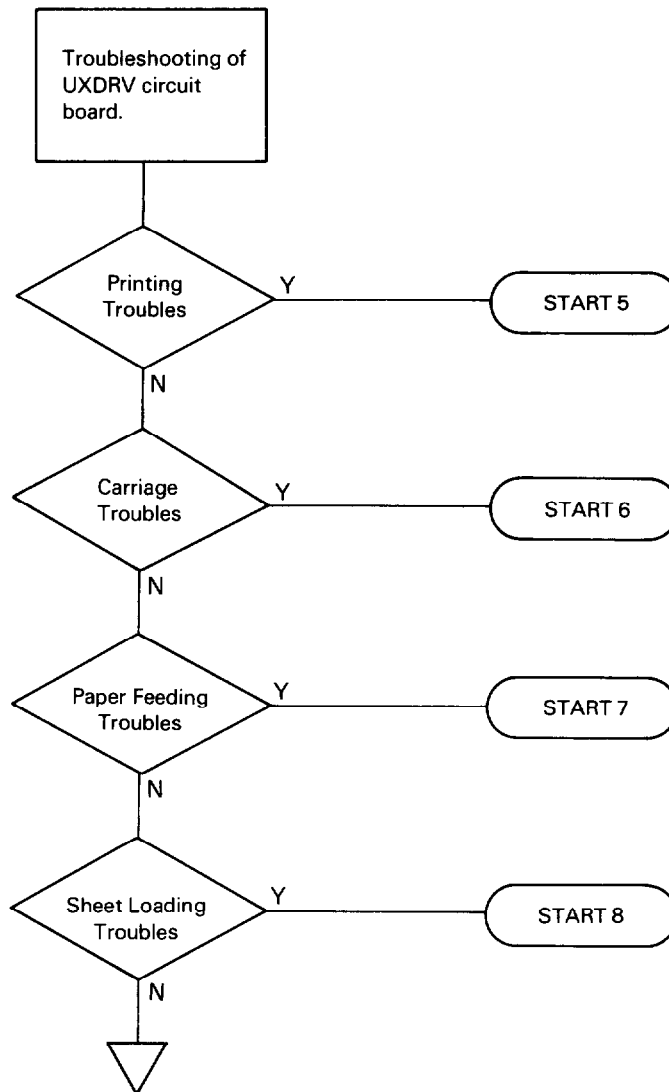




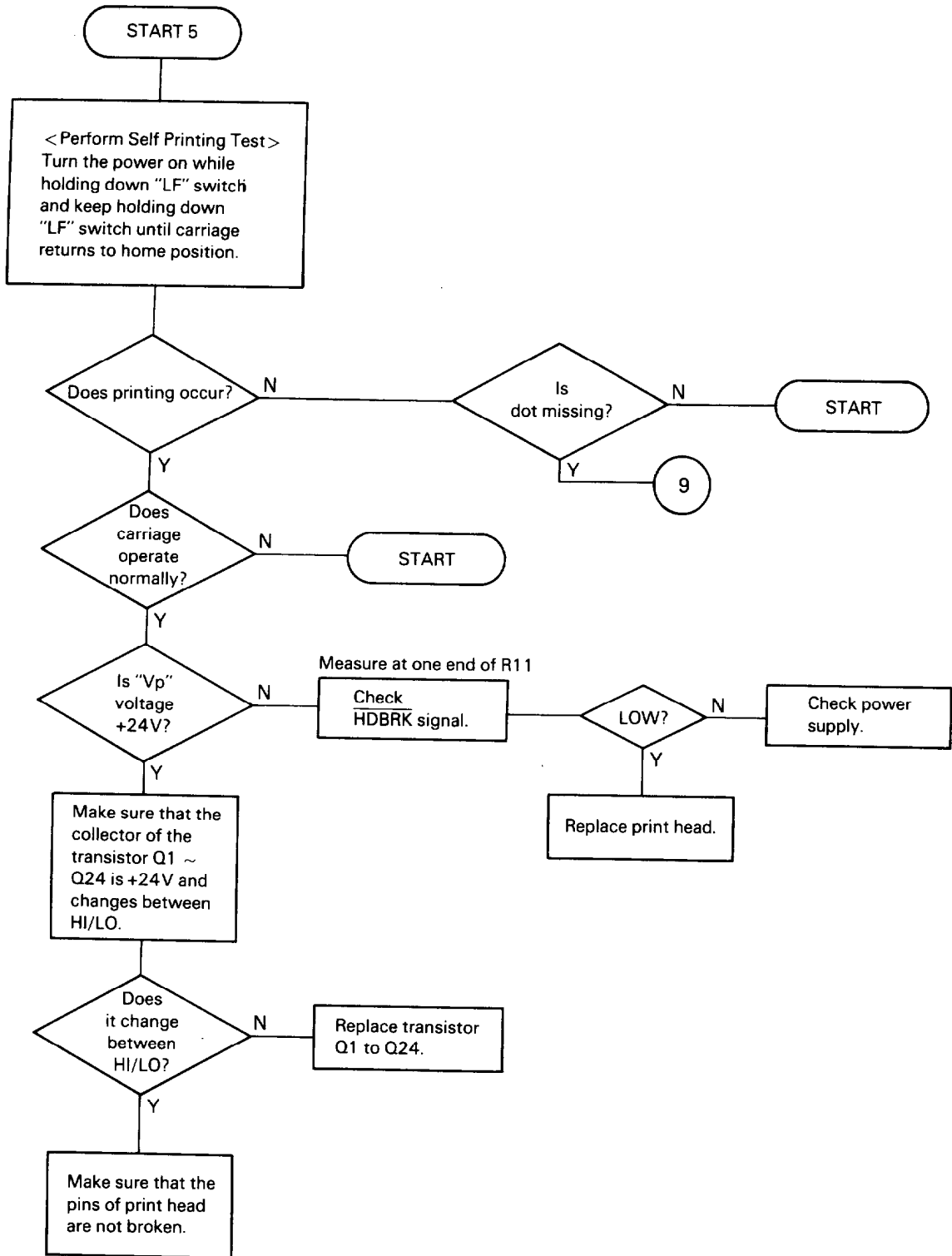
4. Sheet Loading Problem

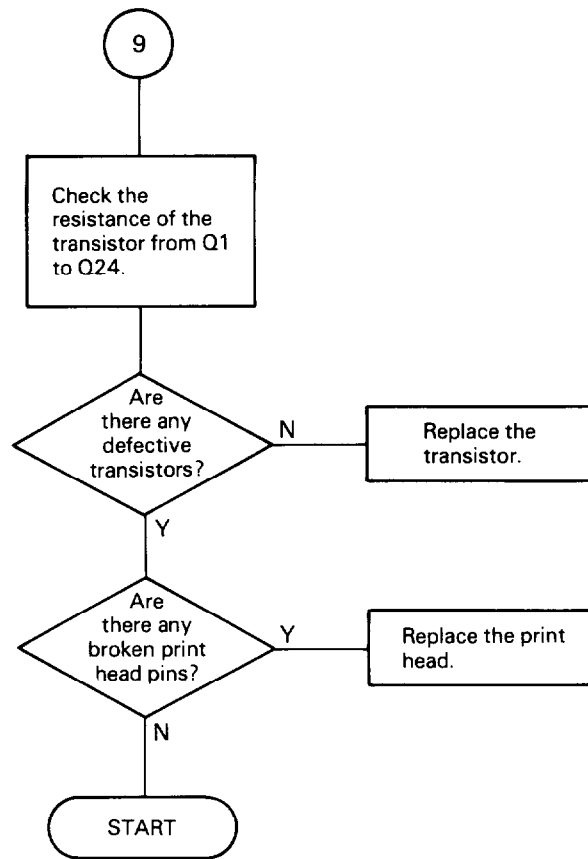


5.4 Unit Repair Flow Chat-t (UXDRV)



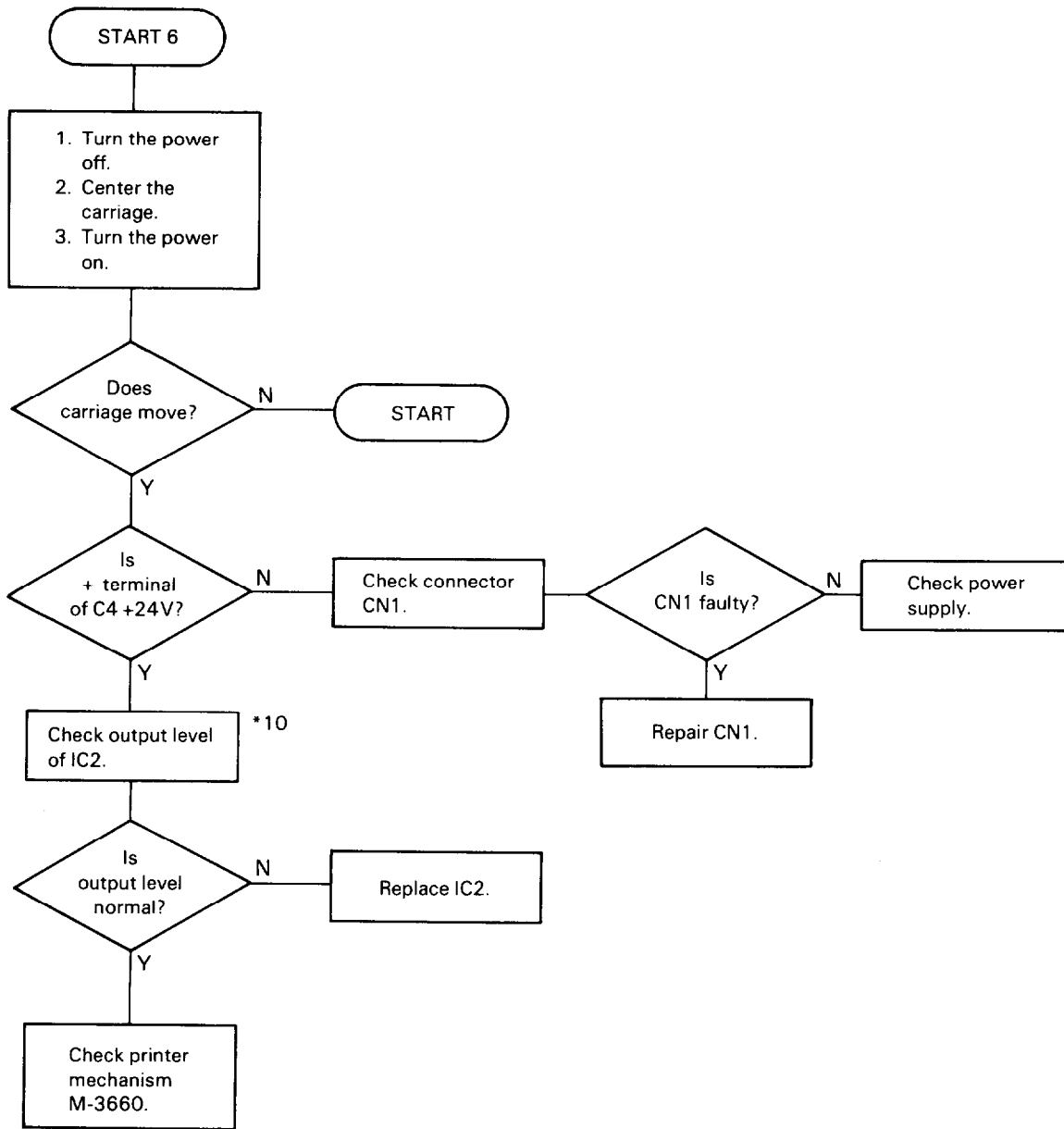
1. Printing Troubles





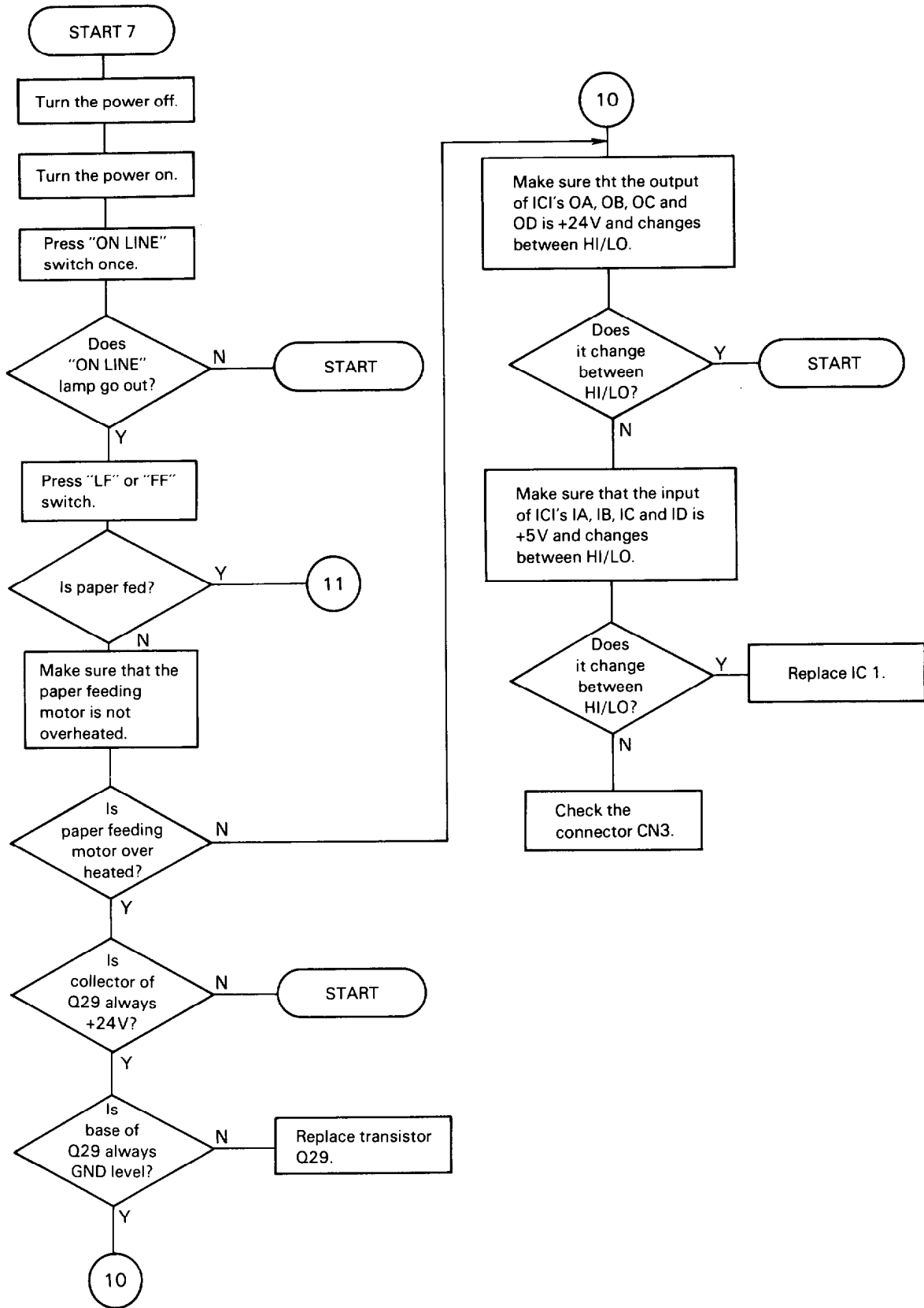
Tested Lead		Resistance
+	-	
Emitter	Collector	∞
Collector	Emitter	Approx. 38Ω
Base	Collector	∞
Collector	Base	Approx. 40Ω
Emitter	Base	Approx. 220Ω
Base	Emitter	Approx. $5k\Omega$

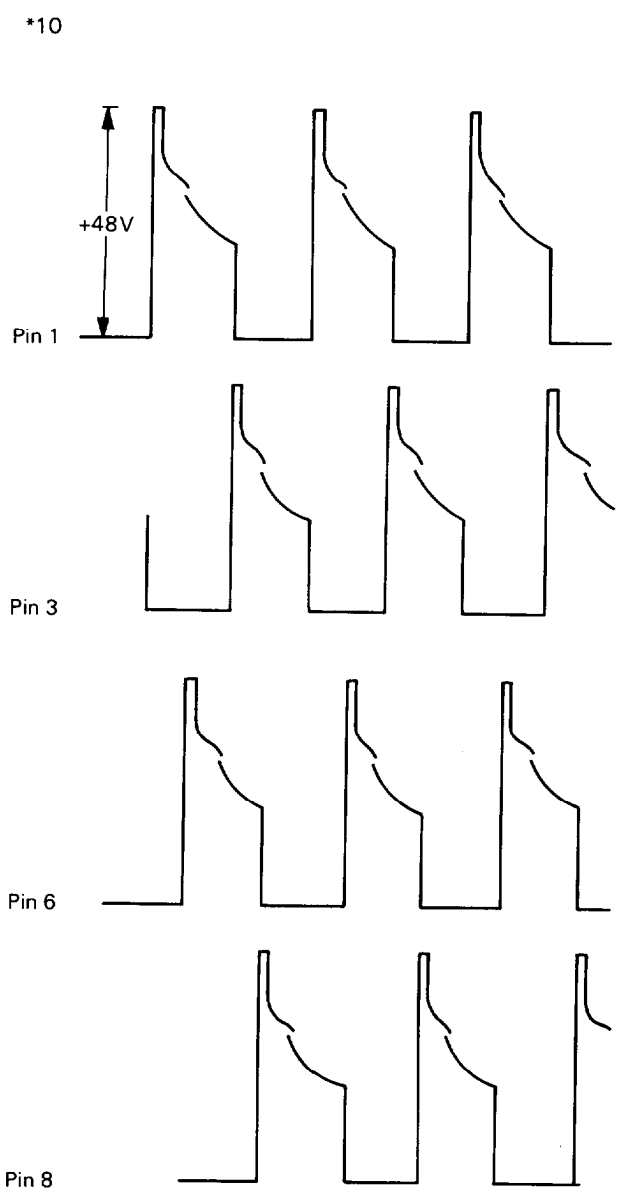
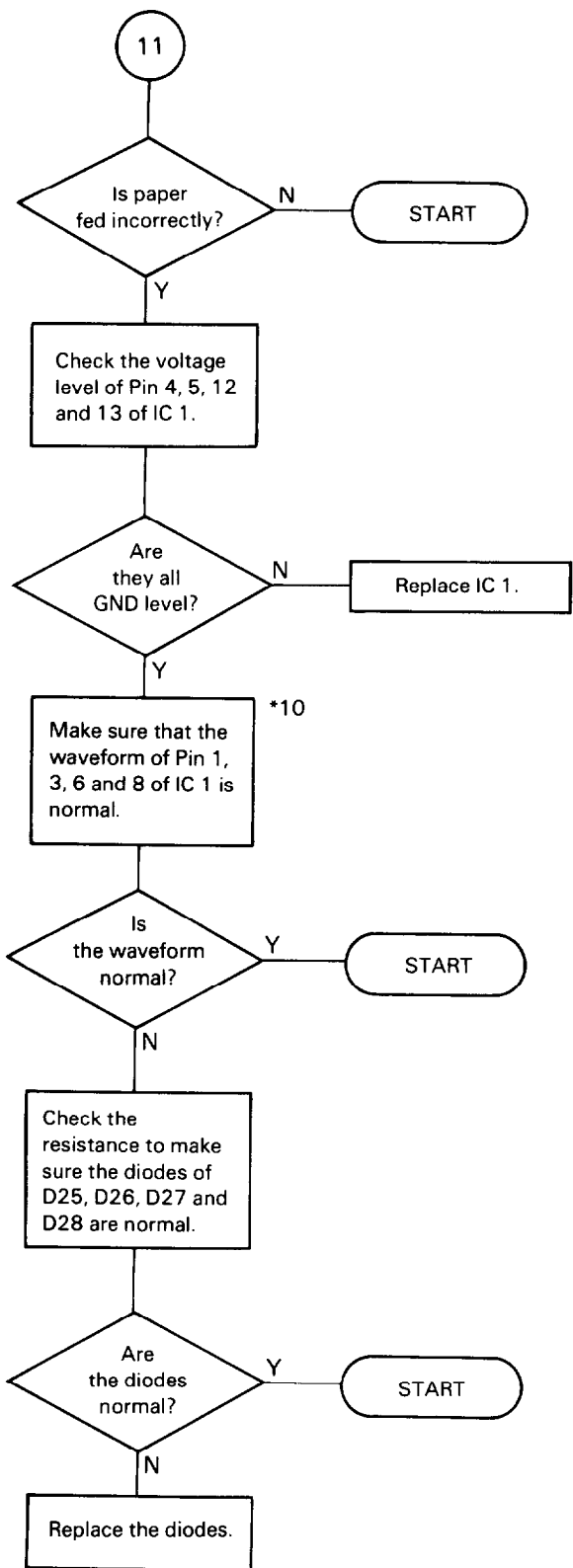
2. Carriage Troubles



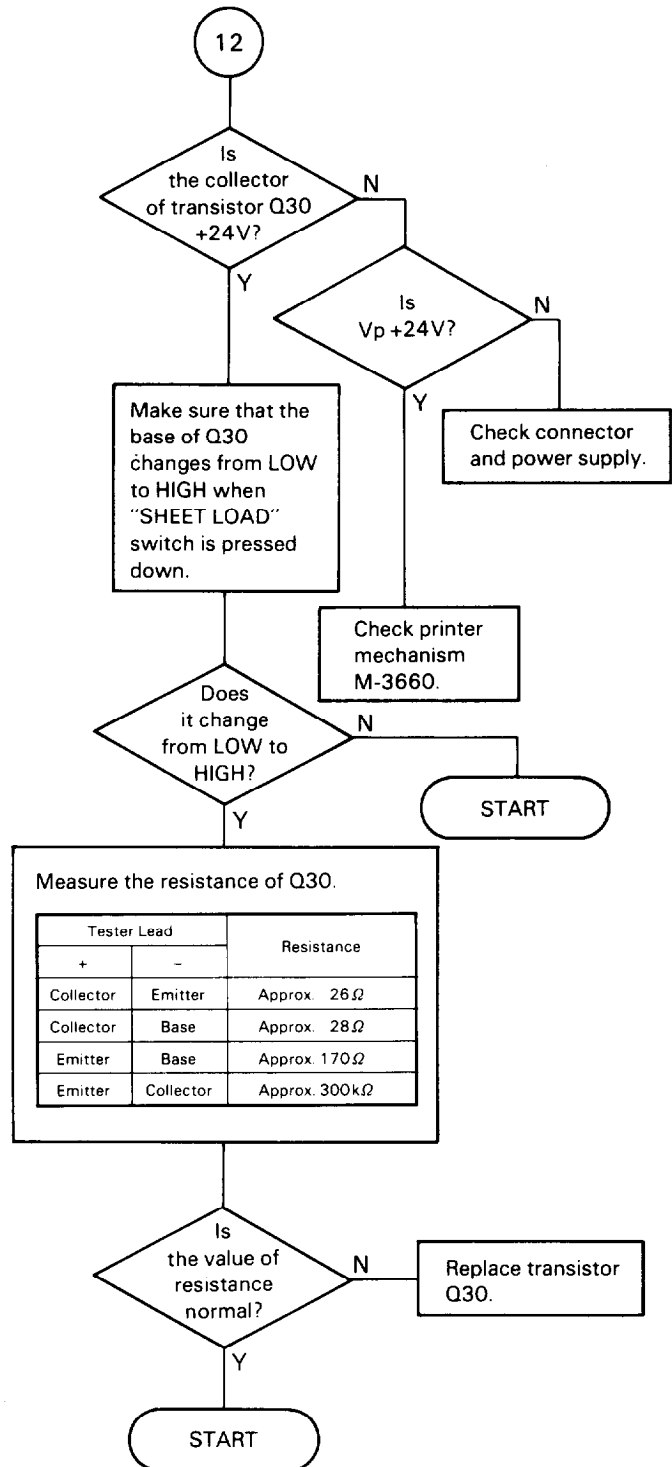
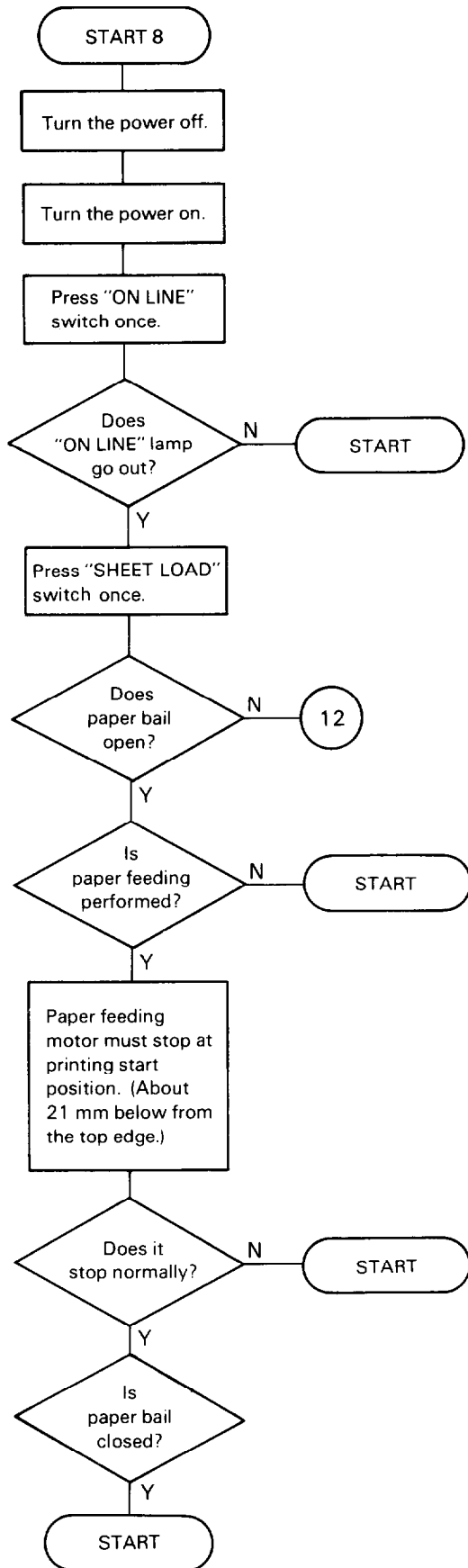
*10 See page 5-28.

3. Paper Feeding Troubles

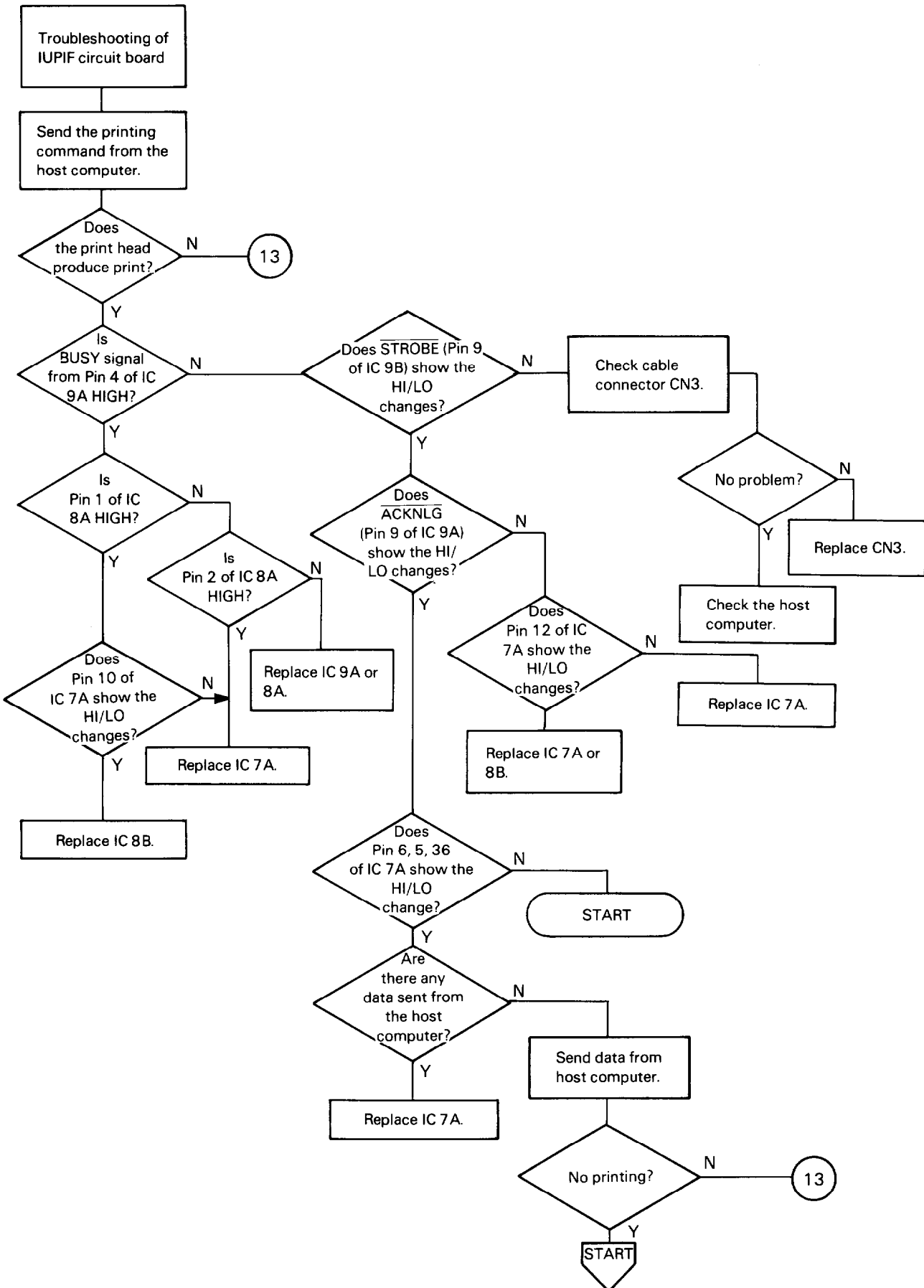


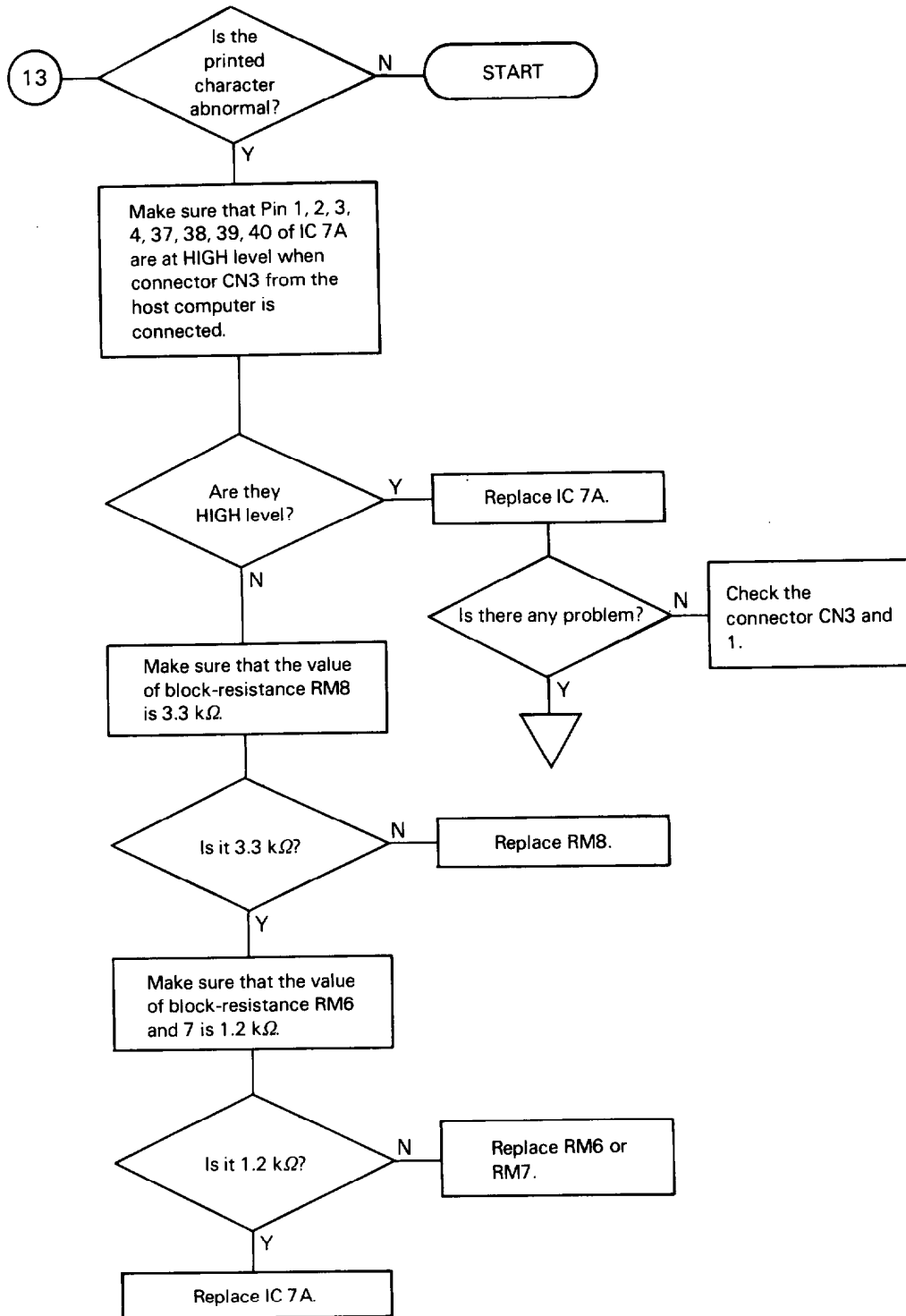


4. Sheet Loading Troubles

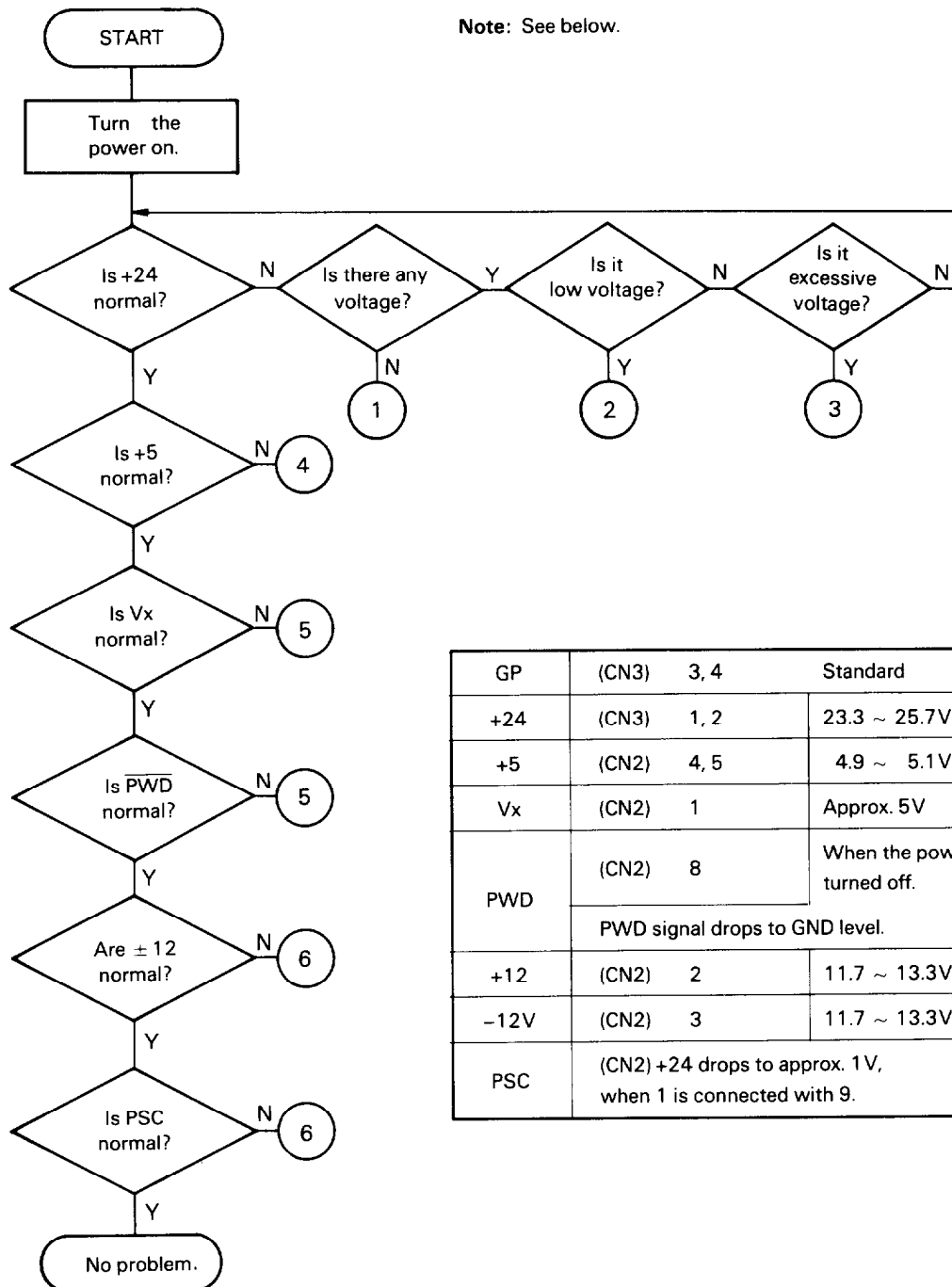


5.5 Unit Repair Flow Chart (IUPIF)





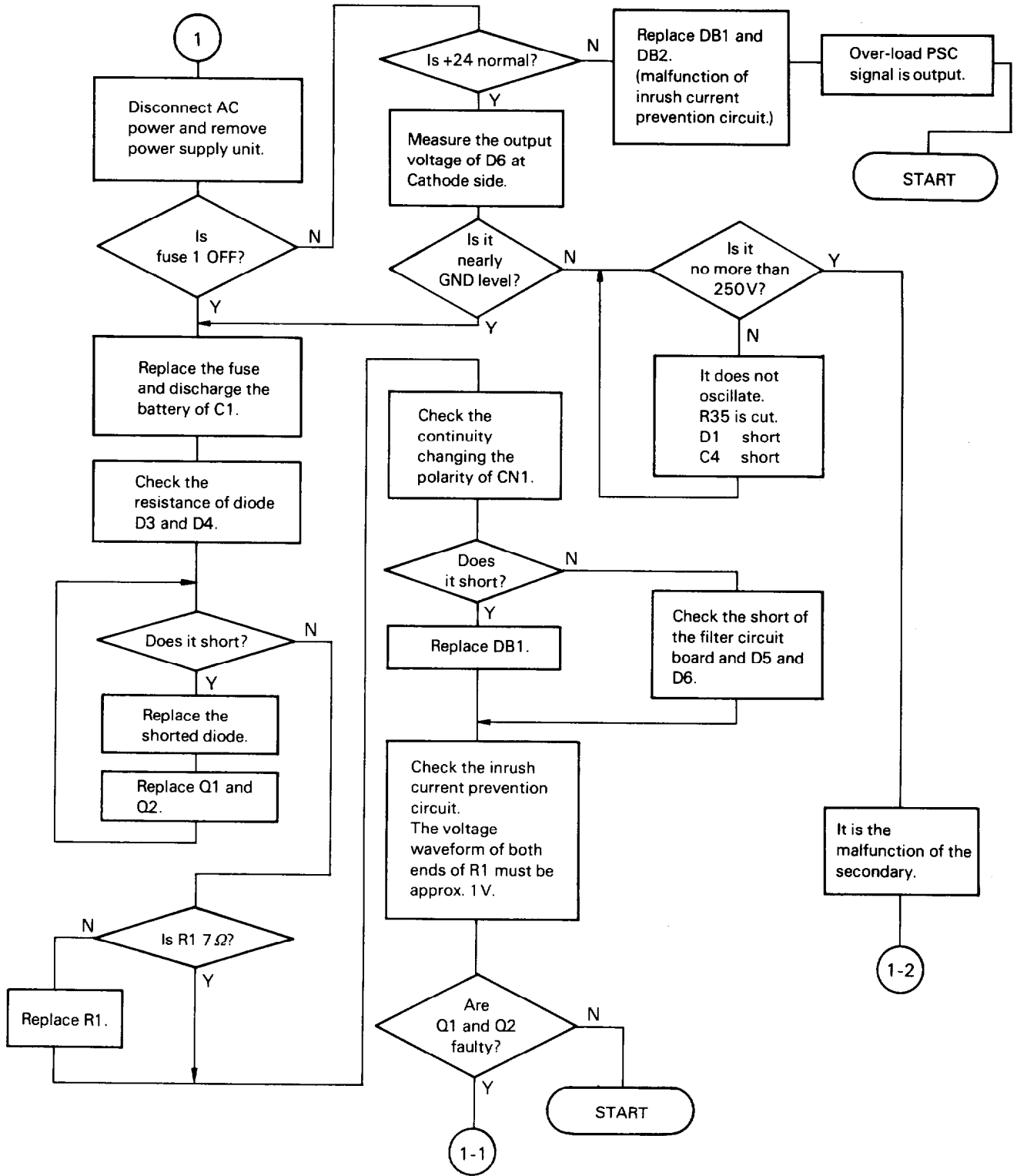
5.6 Unit Repair Flow Chart (UXPS)



Notes:

1. Repair problem by disconnecting the load.
2. ± 12V source will drop down approx. 5V at no load condition.
3. When exchanging any part, be sure to disconnect the A.C cable from the power source.
4. Do not operate the oscilloscope while its ground wire is connected to the earth.

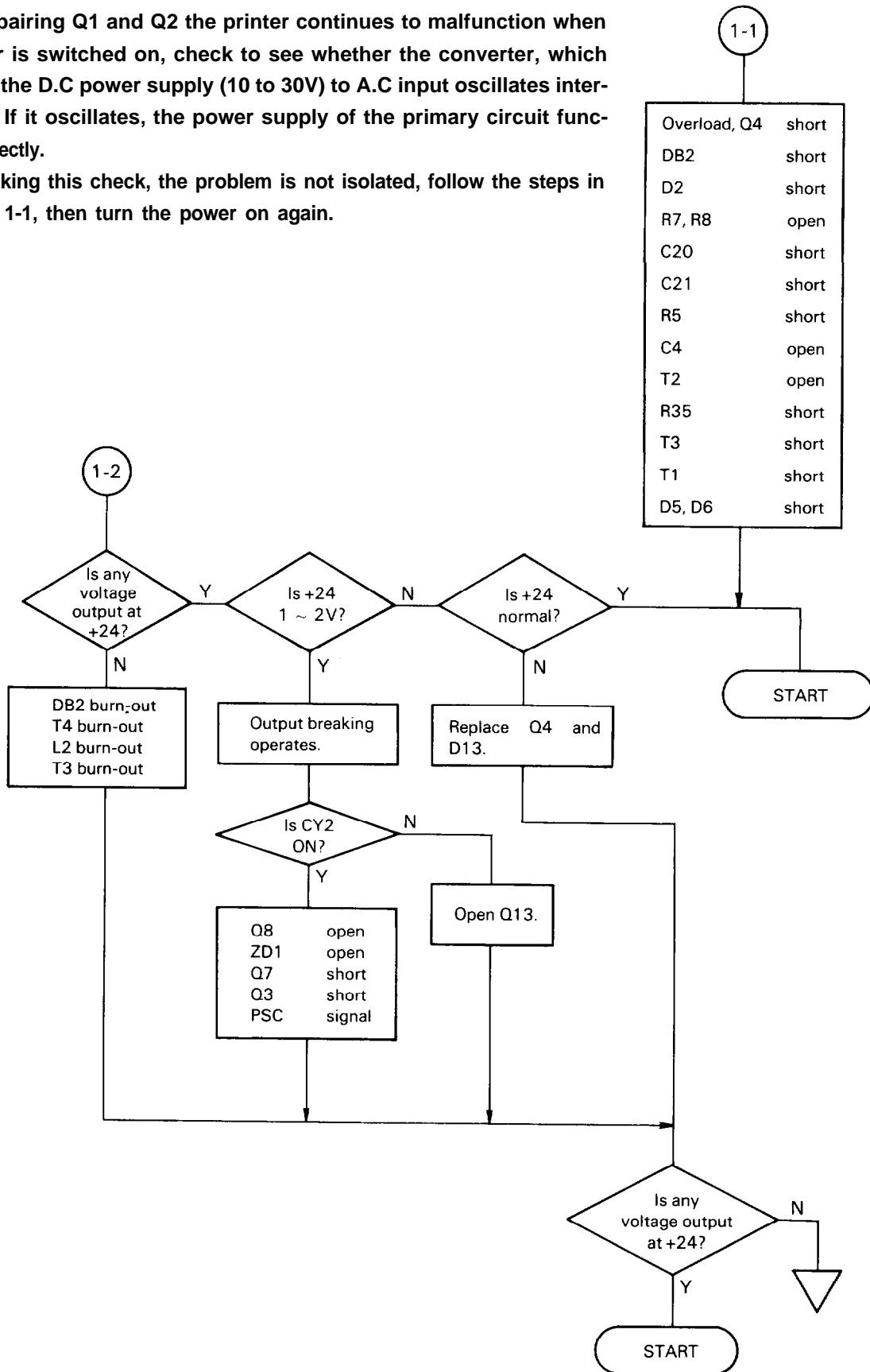
+24 voltage is not output. (The malfunction of the primary.)



The cause of Q1, Q2 malfunction

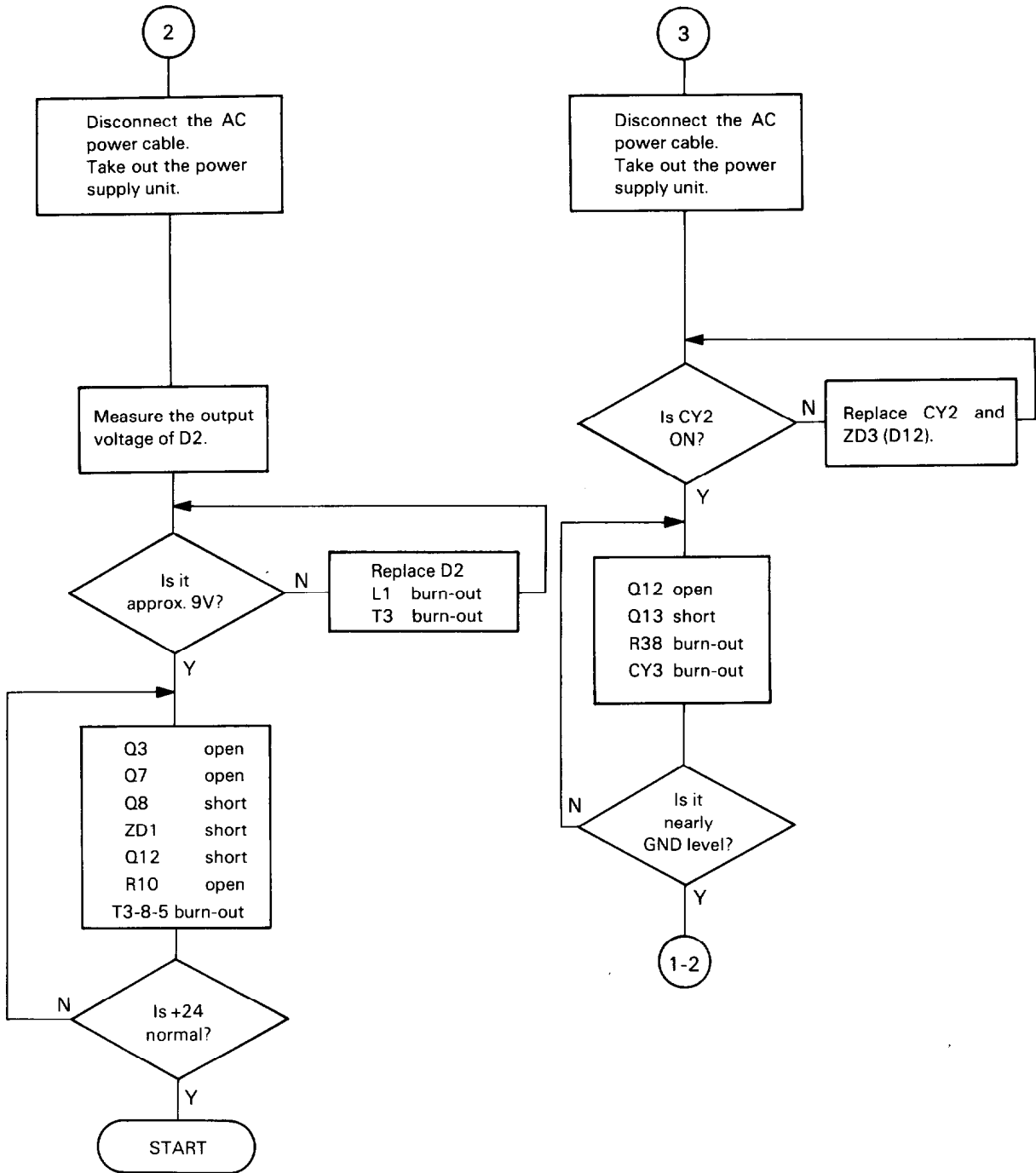
If after repairing Q1 and Q2 the printer continues to malfunction when the power is switched on, check to see whether the converter, which connects the D.C power supply (10 to 30V) to A.C input oscillates intermittently. If it oscillates, the power supply of the primary circuit functions correctly.

If after making this check, the problem is not isolated, follow the steps in flow chart 1-1, then turn the power on again.

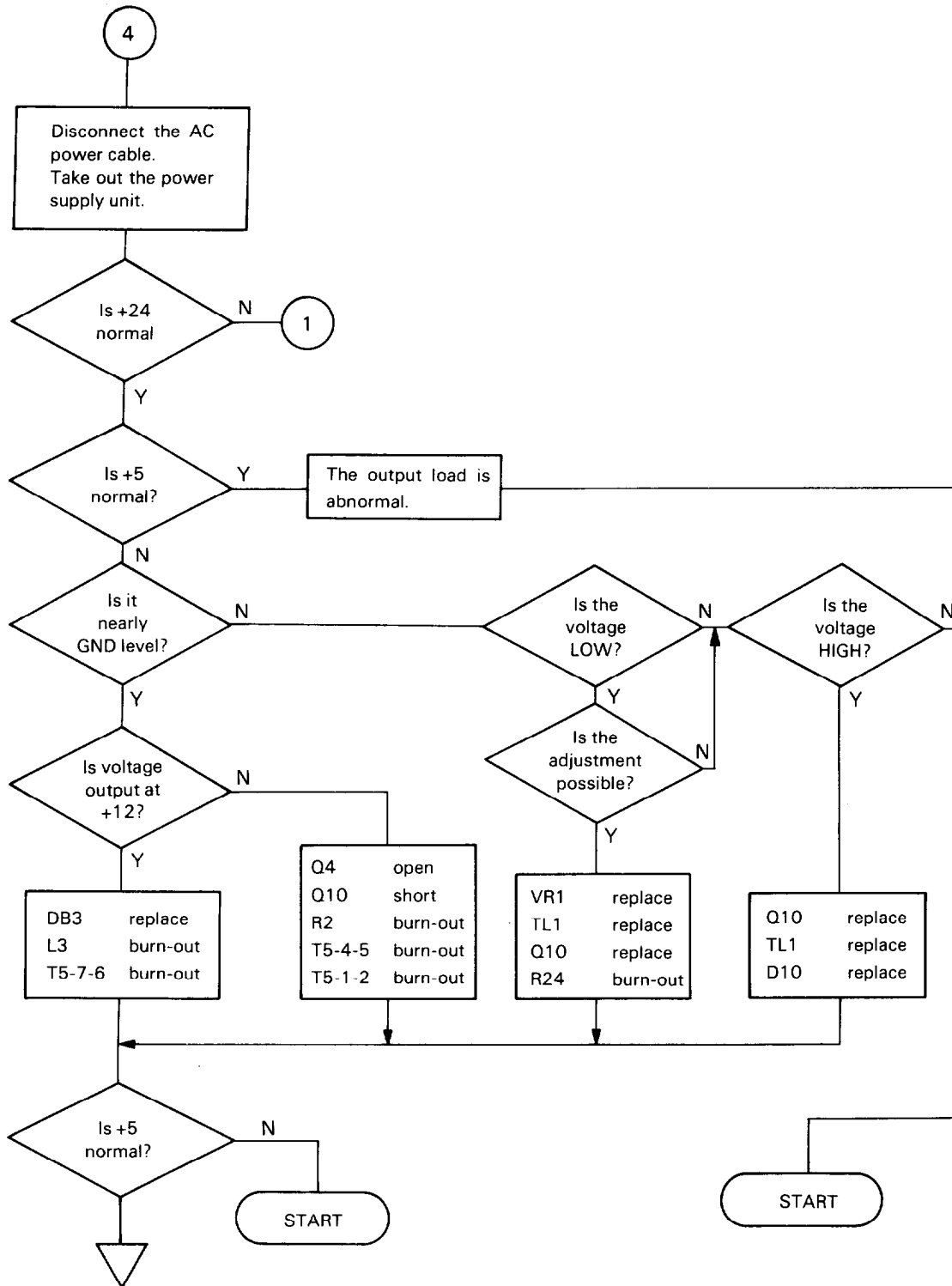


The voltage of +24 is low.

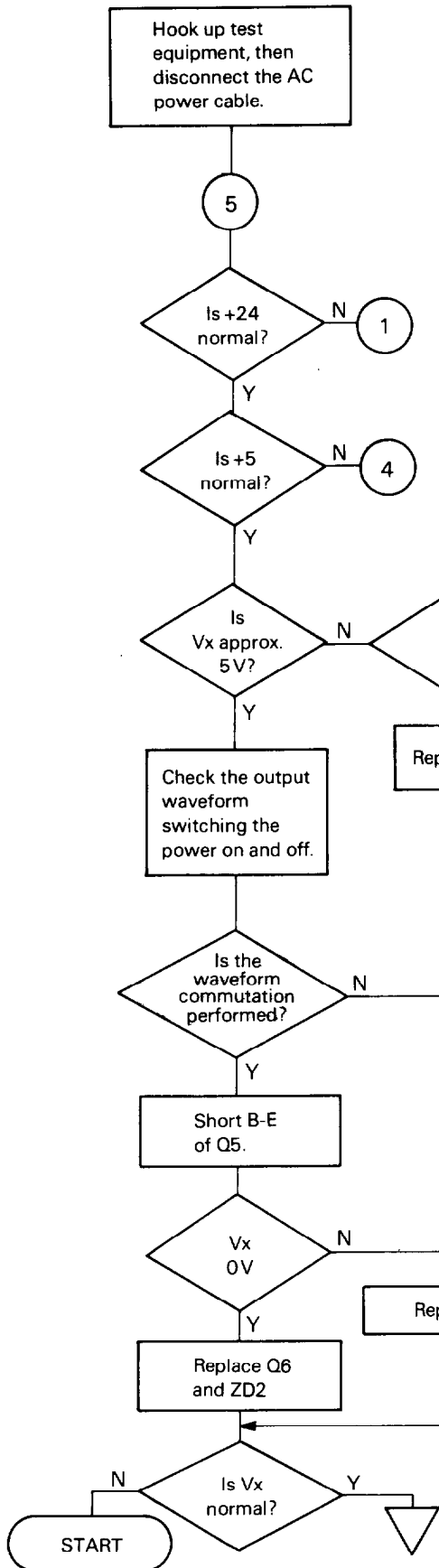
Excessive voltage is output.



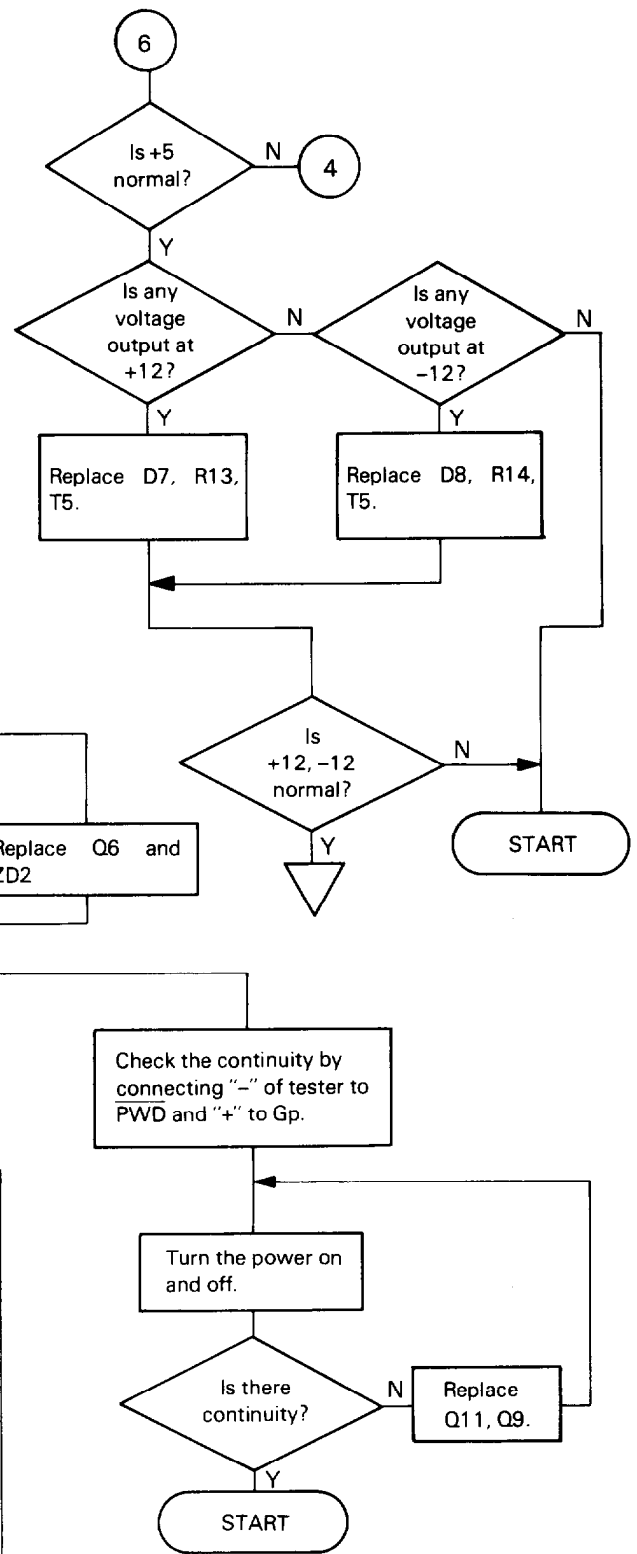
+5 is abnormal.



Vx is abnormal.



12 is abnormal.



CHAPTER 6 MAINTENANCE

6.1	Maintenance	6-1
	6.1.1 Cleaning	6-1
	6.1.2 Inspection..	6-1
6.2	Lubrication..	6-2
	6.2.1 Lubricants..	6-2
	6.2.2 Lubrication requirement..	6-2
	6.2.3 Lubrication point..	6-2
	6.2.4 Adhesive application requirements..	6-3
	6.2.5 Adhesive application points..	6-3
	6.2.6 Lubricants and adhesives list..	6-4

6.1 Maintenance

Proper maintenance is essential for the printer to keep its designed performance for the longest possible period, and to minimize the frequency of trouble. Carry out maintenance according to the following instructions.

6.1.1 Cleaning

(1) Remove any dirt or stains using alcohol.

Note: Never use thinner, trichloroethylene or ketone-based solvents, which might deteriorate plastic parts.

(2) Remove paper particles and dust.

To remove any paper particles and dust from the surface and inside of the printer, it is recommended that a vacuum cleaner be used.

Note: After cleaning, check the lubrication points for quantity of lubricant. Resupply the specified lubricant, as required. (Refer to Par. 2.4 Lubrication Requirements.)

6.1.2 Inspection

Inspection of the printer divides into the following categories:

(1) Daily inspection:

This can easily be carried out by the operator of the printer. As part of his routine work, the operator should check if the printer is properly used and see to it that the printer may serve in the best condition.

● Check points:

- ① Check if the paper is not caught around or by the paper feed box, the printer casing or other objects.
- ② Check if the cassette ribbon is set in position (see Fig. 2.1).
- ③ Check if dusts or other foreign materials are not found in the printer.

(2) Periodic inspection:

This can be carried out only by persons who are familiar with the operating principle and mechanisms of printers. Have the printer inspected and lubricated by such persons every six months or each time 1,000,000 lines have been printed.

● Check points:

- ① Clean carriage shafts A and B, and apply lubricant 0-2.
- ② Clean the gears of the carriage, and apply lubricant G-14.
- ③ Check the springs and ribbon driving wire for deformation or damage.
- ④ Check if the cassette ribbon is properly set in position.
- ⑤ Check the dot head/platen distance (refer to Par. 2.1.3).
- ⑥ Remove paper particles, dust, and other foreign materials (from or around the HP sensor and surrounding components).

6.2 Lubrication

Proper lubrication is essential for the printer to keep its designed performance for the longest possible period, and to minimize the frequency of trouble. Carry out lubrication according to following instructions:

6.2.1 Lubricants

The properties of lubricants used have a great influence on the performance and durability of the printer. In particular, attention must be paid to the low temperature characteristics. It is strongly recommended to use only those lubricants that we have selected after extensive study of technical information and a series of tests on many types of lubricants.

We can supply such lubricants in a metallic can or a plastic container of 40 cc (40 gr), which is the minimum supply unit available.

6.2.2 Lubrication requirements

The lubricants to be used for the printer are G-I 4 and 0-2. Whenever disassembling and reassembling the printer, supply the specified quantity of appropriate lubricant to the lubrication points according to the list below or the lubrication and adhesive application points drawings. (The numbers given in the list correspond to those given in the drawing.) Be sure to thoroughly clean the elements or parts concerned prior to application of lubricant.

The required frequency of periodic lubrication is as follows. When the lubricant is removed by cleaning or when the printer is disassembled or its parts are replaced, be sure to lubricate irrespective of the time set for periodic lubrication.

A) Every six months or each time 1,000,000 lines have been printed.

B) Every occasion of overhaul or each time 5,000,000 lines have been printed.

6.2.3 Lubrication points

(Refer to "Lubrication and Adhesive Application Points Drawing")

* For (1) to (I 0), lubrication is necessary while assembling.

Ref. No.	Lubrication application points drawing	Lubrication point	Lubricant	Required frequency
(1)	A	Contacting parts of paper feeding lever and paper feeding roller assy	G-I 4	B
(2)	A	Contacting parts of paper feeding roller holder and paper feeding lever	G-I 4	B
(3)	A	Contacting parts of sub paper holding release lever (on L and R sides) and frame	G-I 4	B
(4)	A	Contacting part of pin of solenoid shaft and sub paper holding lever	G-14	B
(5)	A	Shaft on which release lever is placed.	G-14	B
(6)	B	Ribbon driving shaft	G-14	B
(7)	B	Shaft on which paper feeding reduction gear is placed	G-14	B
(8)	B	Shaft on which paper feeding transmission gear is placed	G-I 4	B
(9)	B	Inside of platen shaft holder (on L and R sides)	o-2	A
(10)	C	Inside of platen shaft holder (on L and R sides)	o-2	A
(1 1)	A	Paper feeding release lever	G-I 4	B
(1 a	A	Contacting parts of paper holding lever (on L and R sides) and frame	G-I 4	B
(13)	A	Contacting parts of paper holding lever (on L and R sides) and frame support shaft B	G-14	B
(14)	A	Contacting parts of paper holding lever (on L and R sides) and paper holding lock lever	G-I 4	B
II 5)	A	Hook part of paper holding lever spring (on Land R sides)	G-I 4	B

Ref. No.	Lubrication application points drawing	Lubrication point	Lubricant	Required frequency
(16)	A	Contacting parts of sub paper holding lever (on L and R sides) and caulking shaft of paper holding lever	G-14	B
(17)	A	Contacting parts of sub paper holding lever (on L and R sides) and hook shaft for paper guide support spring on frame	G-14	B
(18)	A	Contacting parts of sub paper holding lever (on L and R sides) and frame support shaft B	G-14	B
(19)	A	Contacting part of sub paper holding lever (on L side) and paper holding lock lever	G-14	B
(20)	A	Contacting part of paper holding lock lever and caulking shaft of frame	G-14	B
(21)	A	Retaining ring TYPE-E which fixes belt driven pulley	G-14	B
(22)	B	Teeth of platen gear (one-third perimeter)	G-14	B
(23)	B	Teeth of paper feeding reduction gear (one-third perimeter)	G-14	B
(24)	B	Contacting part of belt driving pulley and motor pinion of belt motor (one-third perimeter of pulley)	G-14	B
(25)	B	Felt (on L and R sides)	O-2	A
(26)	B	Retaining ring TYPE-E which fixes planetary pinion	G-14	B
(27)	B	Teeth of ribbon driving gear (one-third perimeter)	G-14	B
(28)	B	Carriage shaft A	O-2	A
(29)	B	Adjusting lever	G-14	B
(30)	C	Teeth of sprocket gear (one-third perimeter)	G-14	B
(31)	C	Teeth of sprocket transmission gear (one-third perimeter)	G-14	B
(32)	C	Retaining ring TYPE-E which fixes sprocket transmission gear	G-14	B

6.2.4 Adhesive application requirements

This printer contains some screws and nuts secured by adhesive to prevent loosening due to vibrations. During disassembly/reassembly or parts replacement, apply adhesive to the required points according to the list below or "Lubrication and Adhesive Application Points Drawing".

The adhesive to be used for the printer is Neji Lock Green # 2.

6.2.5 Adhesive application points

(Refer to "Lubrication and Adhesive Application Points Drawing")

Note: Use of excessive quantity of adhesive may cause malfunction of adjacent parts due to flow of adhesive, so pay attention to application quantity. (See Fig. 6.1)

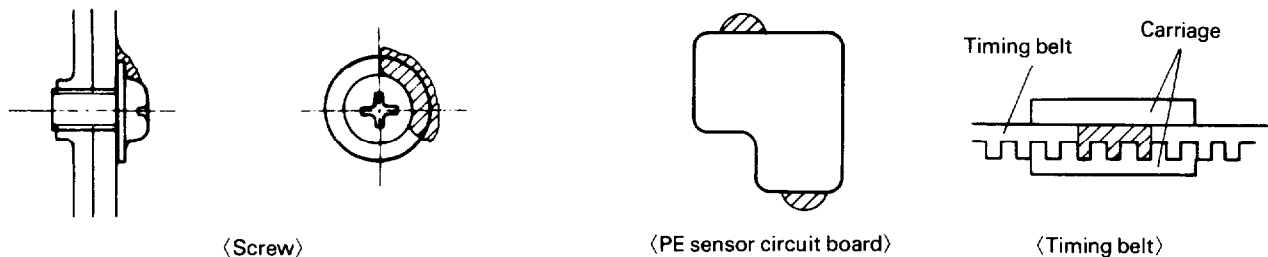


Fig. 6.1

6.2.6 Lubricants and adhesives list

The lubricants and adhesives which are indispensable for maintenance and repair are given below.

Product	Designation	Supply unit	Availability (*)
Oil	O-2	40 cc	Ⓔ
Grease	G-14	40 gr	Ⓔ
Adhesive	Neji Lock # 2 (G)	1,000 gr	○

(○) 0: Commercially available.

Ⓔ: Available only from EPSON.

CHAPTER 7

APPENDIX

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List of Principal IC's

Table 7.1

Name of IC	Parts code	Page
μ PD780C-1 (Z-80)	X400000800	7-2
μ PD8042/8742	Y450800801	7-15
μ PD8041/8741	Y450800802	7-15
μ PD8259AC	X400082591	7-19
μ PD8255AC-5	X400082550	7-20
μ PD7811 (7810)	X400078100	7-21
μ PB6101-009	Y450801001	7-27
8253-5	X400082530	7-28
NE555	X440095550	7-28
NJM2903 (LM-2903)	X440072920	7-29
μ PB8216C/D	X400082160	7-29
8243	X400082430	7-30
27128		7-31
STK6982	X440759820	7-32
HA13007	X440170070	7-33
μ PA79C	X440150790	7-34

Technical Data of Z-80A CPU

1. Architecture Configuration

Fig. 7.1 shows a block diagram of the Z-80A architecture. An chip circuitry fun.

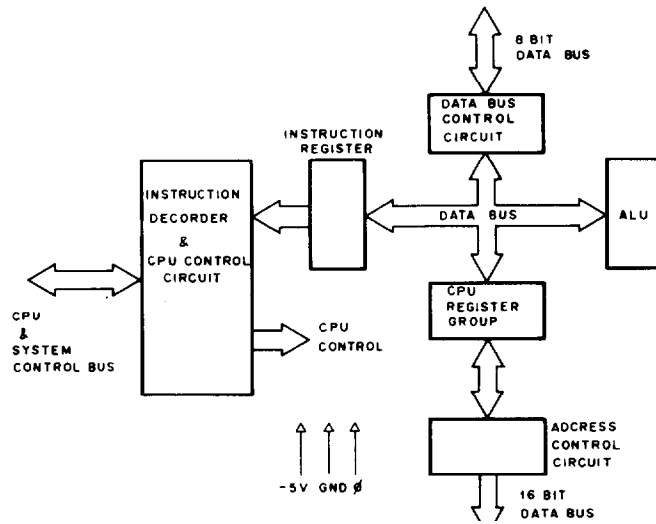


Fig. 7.1

1.1 CPU register group

The Z-80A CPU has a 207-bit read/write memory which can be accessed at random by the program. Table 7.1 indicates the register array of this memory. The array is formed of 16 8-bit registers and 4 16-bit registers, any of which is a static RAM.

Two sets of 6, general-purpose registers, a total of 12 registers are provided on the chip. Each register can be used as a single 8-bit register, or paired to form a 16-bit register.

Other registers on the chip include 2 sets of accumulators and 2 sets of flag registers.

Main resister set

Sub resister set

Accumulator	Flag	Accumulator	Flag
A	F	A'	F'
B	C	B'	C'
D	E	D'	E'
H	L	H'	L'

Table 7.1

Interrupt vector I	Memory refresh R
Index register IX	
Index register IY	
Stack pointer SP	
Program counter PC	

Fig. 7.2

Exclusive registers

1) Program counter (PC)

The program counter holds 16 memory address bits for the instruction being currently executed. The CPU fetches the instruction from the memory address indicated by the program counter. This counter is automatically incremented when its own contents are transmitted to the address bus. In program jump, the increment does not work and a new value is set directly to the counter.

2) Stack pointer (SP)

The stack pointer holds 16, high-order address bits in the stack of an external RAM. An external stack is formed of a LIFO (last-in, first-out) file.

The data is transferred from the designated register in the CPU to the stack or vice versa on command PUSH or POP.

When the data are taken out (POP) of the stack, the data which has been entered (PUSH) last is removed first. The stack is useful to facilitate multilevel interruption, limitless subroutine nesting or a variety of data processings.

3) Index registers (IX and IY)

Two independent index registers (IX and IY) hold 16-bit reference address for index mode addressing. In this index mode, an index register is used for the reference address for designating the memory area where data is put in or out. In the index addressing command, the addition of 1 byte displacement to the contents of this register indicates an effective address. This displacement is given as an integer with two-complement code.

This addressing mode is widely used in different programs, especially those for which data table is referred to.

4) Interrupt page address register (I)

The Z-80 CPU has a mode in which indirect call (indirect subroutine jump) can be applied to any memory location according to the interruption.

For this purpose, register I is provided. The contents of this register refer to the 8 high-order indirect address bits. The address which meets the equipment which has applied an interruption is assigned to the 8 low-order bits. In this system, the interruption handling routine can be located at any area of the memory dynamically, thus enabling jumping to this routine in a very short access time.

5) Memory refresh register (R)

The Z-80A CPU has a built-in memory refresh counter. Therefore, a dynamic memory can be easily used like a static memory.

This 7-bit register is automatically incremented whenever the instruction is fetched.

The data in this register decodes the instruction fetched by the CPU and is put on the low-order bits of the address bus in synchronism with the refresh control signal while this instruction is executed.

In this refresh mode, the programmer need not take care and the CPU operation has no delay. These are the features of the refresh mode. Data can be loaded in this register (register R) according to the program for testing. However, normally, this should not be used for testing.

During refresh, the contents (data) in register I are output to the high-order 8 bits of the address bus.

Accumulators and flag registers

The CPU has 2 sets of independent, 8-bit, accumulators and, in combination with these, 2 sets of 8-bit flag registers. An accumulator holds the 8-bit result of arithmetic or logical operation. On the other hand, a flag register sets the status of 8-bit or 16-bit operation result, e.g. whether or not the result is equal to zero.

General-purpose registers

The CPU is provided with 2 sets of paired general-purpose registers, each of which can be used as an 8-bit register singly and each pair of which can be used as a 16-bit register pair. BC, DE and HL are given as the one set and, BC', DE' and HL' as the other set.

Depending upon the program, either set of registers is selectable by the exchange instruction for the required work at any point of time.

When a high-speed interruption request is required in the system, it is also advisable to move for refuge promptly the contents of accumulator/flag register pair and general-purpose register set to another pair and other set.

Conversion between routines can be performed just by use of a simple exchange instruction. The interruption service time is thereby greatly reduced, since no interruption or subroutine processing time is needed and it is unnecessary to move or return the register contents to or from an external stack.

These general-purpose registers are usable for a wide range of applications.

When a simple read/write memory is needed for a simple program and especially in a ROM based system, it is advisable to substitute general-purpose registers for it.

1.2 Arithmetic/logic unit (ALU)

The 8-bit arithmetic/logical operation instruction is executed at the ALU inside the CPU.

The ALU is connected to each register through the internal bus to perform data transfer and reception.

The functions related to the ALU are as enumerated below.

Add	(Addition)
Subtract	(Subtraction)
AND	(Logical product)
OR	(Logical sum)
XOR	(Exclusive OR)
Compare	(Comparison)
Shift Left, Right	(Left shift, right shift)
Rotates arithmetic, logical	(Arithmetic rotation and logical rotation)
Increment	(Increment: +1)
Decrement	(Decrement: -1)
Set bit	
Reset bit	
Test bit	

1.3 Instruction register and CPU control

Each instruction is read out from the memory and is held in the instruction register. Then, the instruction is decoded. The control section (CPU) carries out this control and, at the same time, generates the control signal required to read or write data from or to the register group. In addition, this section generates the ALU control signal and necessary external control signal.

2. Pin Functions

The Z-80 CPU is housed in a standard 40-pin DIP (dual in-line package). Its I/O pins are arranged as shown in Fig. 7-2. The following describes each pin function.

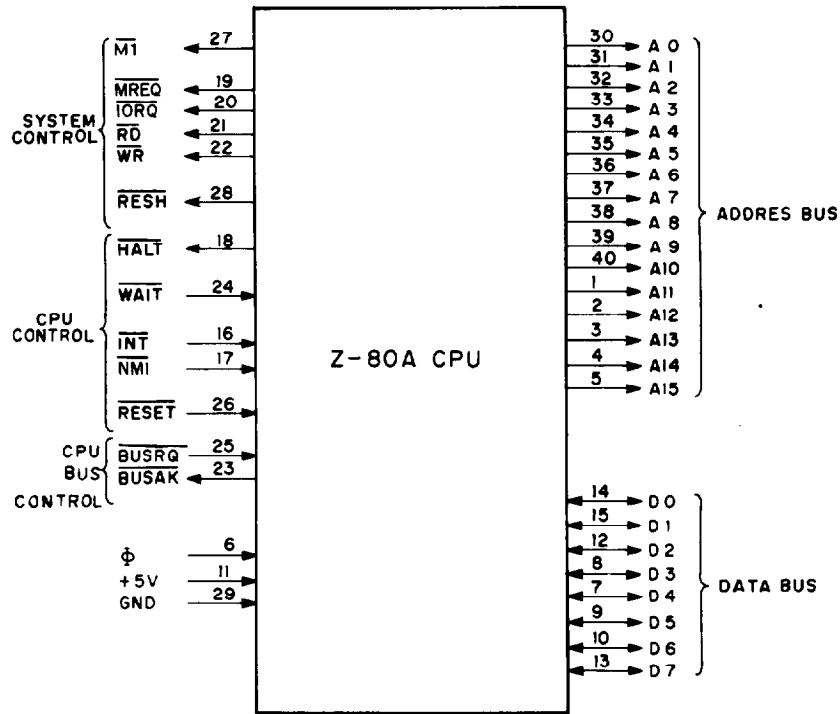


Fig. 7.2 Pin configuration

A₀ – A₁₅
(Address bus)

Tri-state, active HIGH
A₀– A₁₅ form a 16-bit address bus.

This address bus designates the address for data transfer and reception to and from memory (max. 64 K-bytes) and I/O device exchanges. The 8 low-order bits are assigned for I/O addressing. Thus, the user can select from 256 input or output ports directly. In addition, A₀ is LSB (least significant bit). During refresh time, the effective address for refresh is put on the low order 7 bits.

D₀ – D₇
(Data bus)

Tri-state I/O, active HIGH
D₀ - D₇ forms an 8-bit two-way data bus. The data bus is used for data exchange with memory or I/O unit, or between them.

\overline{M}_1
(Machine cycle 1)

Output, active LOW
Signal \overline{M}_1 is emitted when the current machine cycle is the OP code fetch cycle of an instruction execution. It should be noted that when executing a 2-byte OP code, signal \overline{M}_1 is emitted at every fetch cycle of the OP code. For an instruction with a 2-byte OP code, the initial part of the OP code starts with CB_H, DD_H, ED_H or FD_H.

Further, signal \overline{M}_1 is also emitted when interruption is acknowledged. The CPU tells the external unit through \overline{M}_1 and IORQ that interruption is acknowledged.

\overline{MREQ}
(Memory request)

Tri-state output, active LOW.
The memory request signal is emitted when the effective address for memory read or write is put on the address bus.

IORQ (I/O request)	<p>Tri-state, active LOW</p> <p>The I/O request signal is emitted when the effective I/O address for I/O read or write is put on the low-order 8 bits of the address bus.</p> <p>This signal is also emitted together with signal M_i cycle, during an interrupt acknowledged, telling the I/O unit that the interruption response vector can be put on the data bus.</p> <p>During the emission of signal M_i, process is not made for the I/O unit but for the interruption acknowledgement.</p>
RD (Memory read)	<p>Tri-state output, active LOW</p> <p>Signal RD is emitted during the time that the CPU can accept data from memory or I/O unit. This signal is used by the addressed I/O to gate the data from the designated I/O unit or memory to the data bus.</p>
WR (Memory write)	<p>Tri-state output, active LOW</p> <p>Signal WR is emitted when the data to be stored in the designated memory or I/O unit is on the data bus.</p>
$\overline{\text{RFSH}}$ (Refresh)	<p>Output, active LOW</p> <p>Signal $\overline{\text{RFSH}}$ is emitted simultaneously with $\overline{\text{MREQ}}$ when the refresh address for dynamic memory is on the low-order 7 bits of the address bus.</p>
$\overline{\text{HALT}}$ (Halt)	<p>Output, active LOW</p> <p>Signal $\overline{\text{HALT}}$ is emitted when the CPU has executed a HALT instruction and requires a maskable (mask enabled) or non-maskable interrupt before resuming operation. During HALT time, the CPU maintains memory refresh by executing NOPs.</p>
$\overline{\text{WALT}}$ (Wait)	<p>Input, active LOW</p> <p>This input signal tells the CPU that memory or I/O unit is not ready to send data.</p> <p>As long as this signal is active, the CPU maintains the wait state. It should be noted that no refresh signal is emitted during this period.</p> <p>Use of this signal enables the CPU to synchronize its operation speed with memory or I/O unit.</p>
INT (Interrupt request)	<p>Input, active LOW</p> <p>The interrupt request signal is emitted from the I/O devices. The interruption enable flag (IFF) is programmed so that when signal BUSRQ is not active, the interrupt request is accepted on completion of the instruction being executed. The CPU emits the acknowledge signal (signal IORQ during M_i signal timing) at the beginning of the next instruction cycle when the interruption is accepted. For details, see chapter 5 (Instruction group to control CPU). Three kinds of interruptions are maskable.</p>

NMI (Non-maskable interrupt request)	Input, leading edge detection The non-maskable interrupt request has a priority order higher than that of the interrupt request (INT). Thus, when this signal enters before the rise of the last T cycle of the instruction being currently executed, it is accepted after completion of this instruction. This has no relation to the status of the interruption enable flag. With signal NMI input, the CPU restarts at address 0066 _H . The contents of the program counter are automatically saved in an external stack so that CPU can return to the interrupted program. When WAIT cycles continue, signal NMI is kept waiting. In addition, $\overline{\text{BUSRQ}}$ is higher than NMI in priority order.
$\overline{\text{RESET}}$ RESET	Input, active LOW With $\overline{\text{RESET}}$ input, the program counter comes to zero and the CPU is initialized. At this time, the following state is entered. 1) Interruption enable flag is reset. 2) Register I is set to 00 _H . 3) Register R is set to 00 _H . 4) Interruption is set to mode 0. During reset, the address bus and data bus have HIGH impedance so that all control outputs become inactive.
$\overline{\text{BUSRQ}}$ BUSRQ (Bus request)	Input, active LOW With the bus request signal, the address, data and tri-state output control buses have HIGH impedance to enable other units to use buses. The moment that the current machine cycle of the CPU ends when $\overline{\text{BUSRQ}}$ becomes active, the buses have HIGH impedance.
$\overline{\text{BUSAK}}$ BUSAK (Bus acknowledge)	Output, active LOW This signal is emitted to the request unit when the address, data and tri-state output control buses have HIGH impedance to enable other units to use buses.
ϕ	Single-phase TTL level clock pulse input terminal.

3. Timing

In a combination of basic operations in the Z-80A CPU, the instruction is executed step by step. The basic operations include the following:

Memory read/write, I/O unit read/write, Interrupt, Acknowledge

Any instruction is executed in a combination of these basic operations. Any of these basic operations, performed with 3 to 6 clock pulses, can be prolonged to synchronize the CPU with an external unit in respect to operation speed. The basic clock pulse period is taken as T cycle and the period of a basic operation as M cycle (machine cycle). Fig. 7.3 shows an example of the array of specific M and T cycles for a particular instruction. In this example, an instruction with 3 machine cycles (M1, M2, M3) is indicated.

The first M cycle is the fetch cycle of an instruction. This fetch cycle is usable in 4, 5, or 6 T cycles. However, with the wait signal (detailed in the next paragraph), this cycle number can be changed. The fetch cycle (M1) is the period to fetch the OP code of the instruction to be executed next.

In a subsequent M cycle, data is transferred between the CPU and a memory or an I/O unit. This M cycle also consists basically of 3 to 5 cycles. However, the cycle number changes with the wait signal which is input to synchronize with an external unit.

An explanation on the timing in a basic machine cycle is given below.

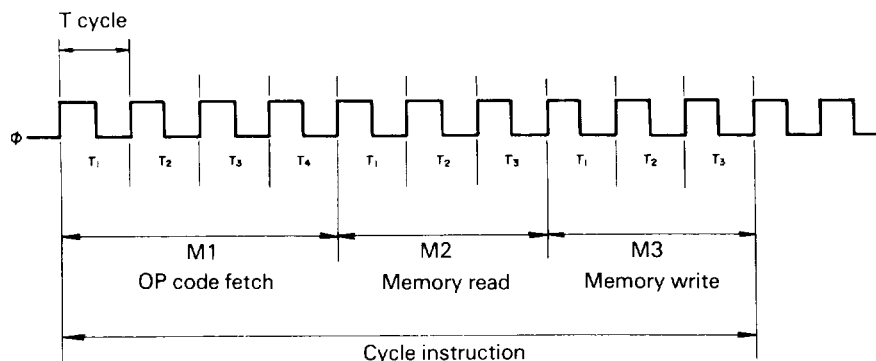


Fig. 7.3

All CPU timings are analyzed as shown in Fig. 7.4 (simplified timing chart). The respective basic operation timing charts with and without the wait signal are shown in the following. (The wait state is applied to synchronize the CPU with a low-speed memory or an low-speed I/O unit.)

3.1 Instruction fetch

Fig. 7.4 is the timing chart in the M1 cycle (OP code fetch). The contents of the program counter are put on the address bus at the head of the M1 cycle and signal MREQ becomes active in the half cycle of clock pulse. At this time, as the address signal to the memory is already stable, the trailing edge of signal MREQ is directly usable for the chip enable clock pulse to a dynamic memory.

Signal RD also becomes active to indicate that the data to be read from the memory can be put on the CPU data bus. The CPU samples data from memory at the leading edge of clock pulse T₃. At this leading edge, signals RD and MREQ are switched in level. However, the CPU performs data sampling before signal RD becomes inactive.

Clock pulse T3 and T4 in the fetch cycle are used to refresh dynamic memory. (In the period of T3 and T4, as the fetched instruction is decoded and executed within the CPU, no other, operation to external units is made.)

In the period of T3 and T4, the memory refresh address is put on the 7 low-order bits of the address bus and signal RFSH becomes active. This signal instructs to refresh all dynamic memories within this period.

Note that during refresh time, signal RD is not emitted to prevent data from being put on the data bus from any other memory segment.

Signal MREQ during refresh time is used to read the data for refreshing all dynamic memories. The refresh signal cannot be used alone. The reason is that since the refresh address is stable only while signal MREQ is emitted, the two signals must be used together.

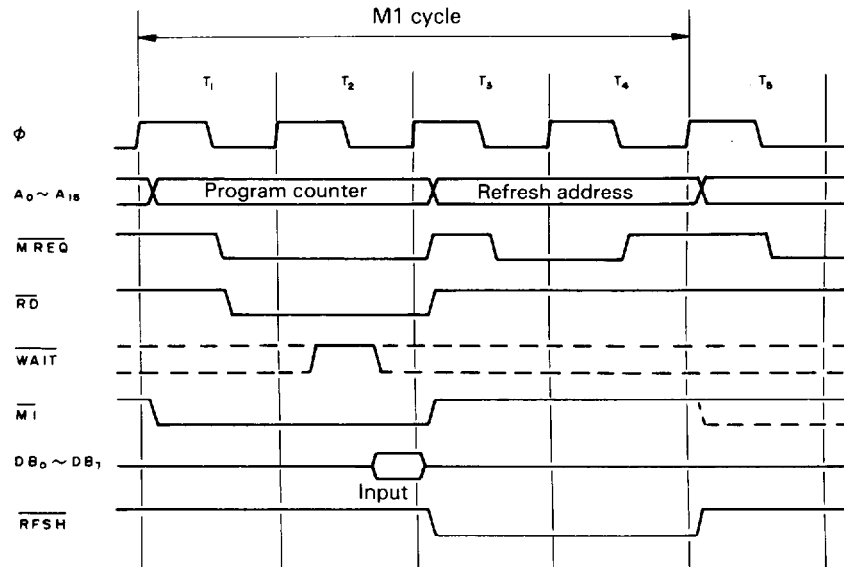


Fig. 7.4

Fig. 7.5 represents the delay of the fetch cycle when the wait signal (\overline{WAIT}) is included. The CPU samples the wait signal at the respective trailing edges of T2 and its following pulses Tw. At this time point of sampling, when the wait signal is active, a further wait state is given at the next T cycle. In this way, the read time is prolonged to control the access time of any type of memory.

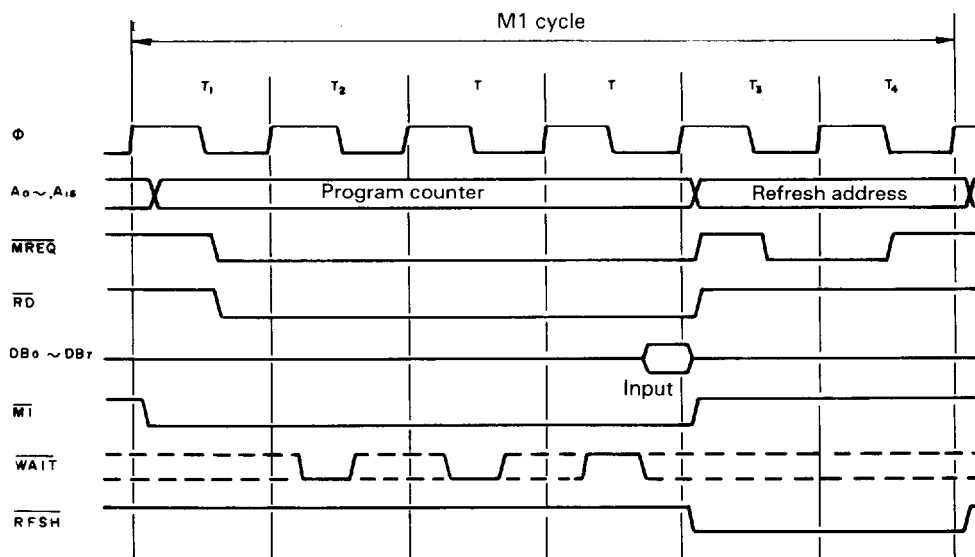


Fig. 7.5

3.2 Memory read/write

Fig. 7.6 is the timing chart for the memory read/write cycle. The memory read/write cycle normally has the length of 3 T cycles, unless the wait signal emitted from the memory side is given. Signals MREQ and RD are used in the same way as in the fetch cycle.

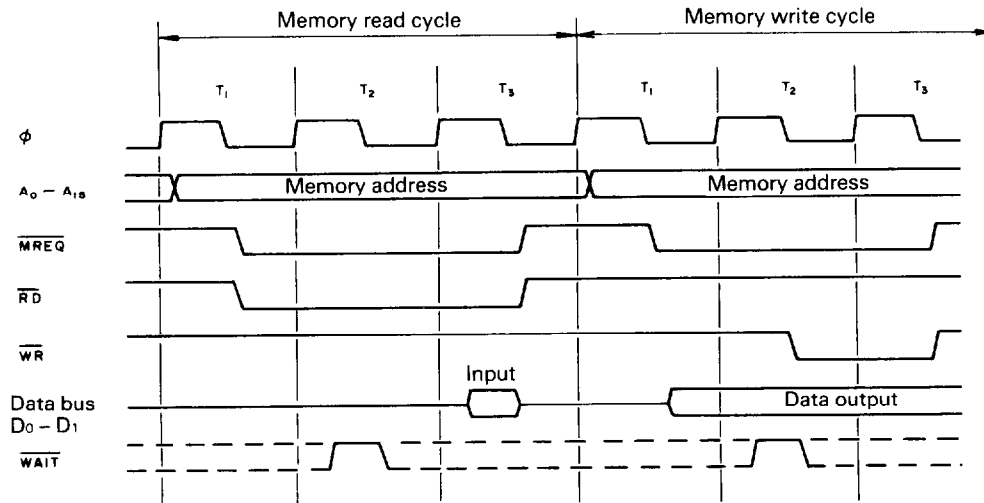


Fig. 7.6

In the memory read/write cycle, as signal MREQ becomes active when the address bus becomes stable, this signal can also be used directly for the chip enable pulse to the dynamic memory.

As signal WR becomes active when the data bus becomes stable, it can also be used for the memory read/write pulse directly.

In practice, signal WR is usable for the read/write signal of almost all types of semiconductor memories. Furthermore, signal WR becomes inactive at the center of the T cycle before the T cycle at which the contents of the data bus change. Therefore, in practice, this signal is usable without problem even in the overlap condition of any type of semiconductor memory.

Fig. 7.7 shows the timing chart when the wait signal (\overline{WAIT}) is present in the memory read or write operation.

This operation is the same as that described in paragraph 3.1 (fetch cycle). In practice, although the memory read and write cycles do not appear concurrently, they are shown here on the same diagram for convenience.

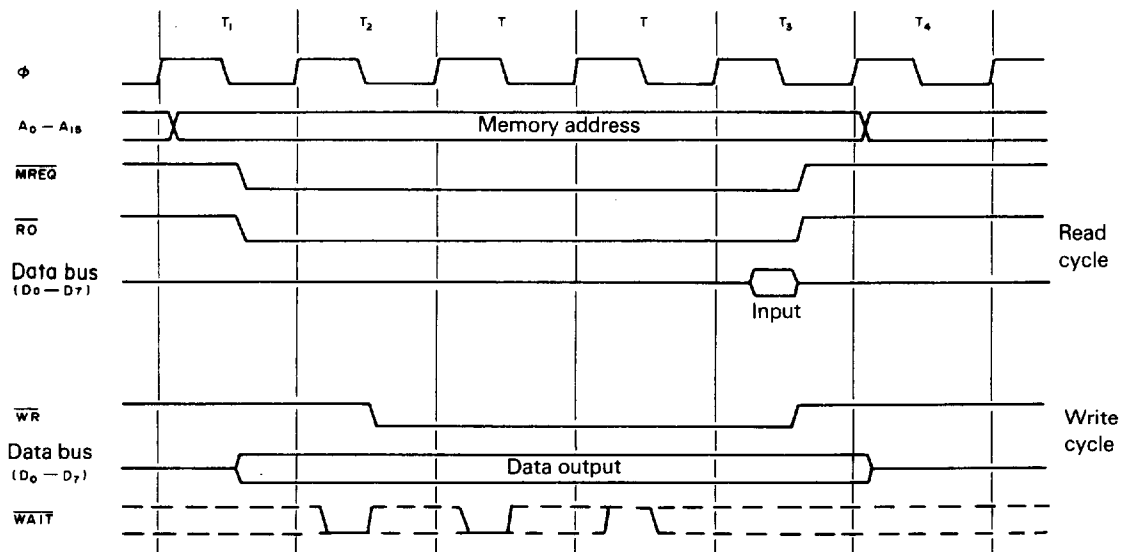


Fig. 7.7

3.3 I/O cycle

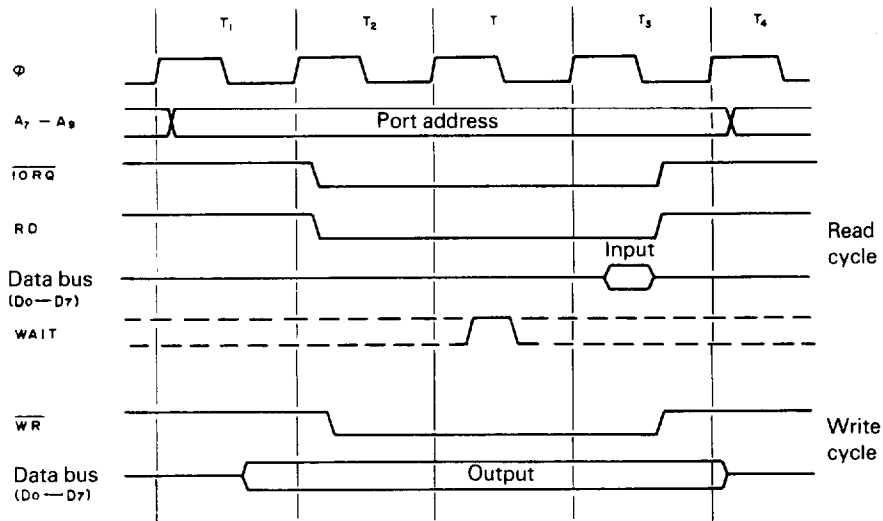
Fig. 7.8 indicates the read and write operations to I/O units. In this case, it should be noted that one wait state of T_w cycle is inserted automatically to compensate for the brief time required for the CPU to sample data after \overline{IORQ} becomes active. This period is not sufficient for the I/O process T_w unless the wait signal is implemented after decoding the port address.

In addition, unless this wait state is given, it is difficult to operate the CPU at the highest speed with MOS I/O units built in.

The wait signal is sampled in the period of T_w . As in memory read operation; it is also advisable in I/O read operation to use signal \overline{RD} to connect the designated port to the data bus.

In I/O write operation, signal \overline{WR} is used for the clock pulse to the I/O port. As this signal provides a sufficient overlap time automatically, its leading edge is usable for the data clock pulse.

Fig. 7.9 indicates the position when an extra wait cycle is added with the wait signal entered. This operation is the same as in the previous examples (Fig. 7.4, Fig. 7.5, etc.)



*Wait state (signal pulse T_w) is inserted automatically.

Fig. 7.8

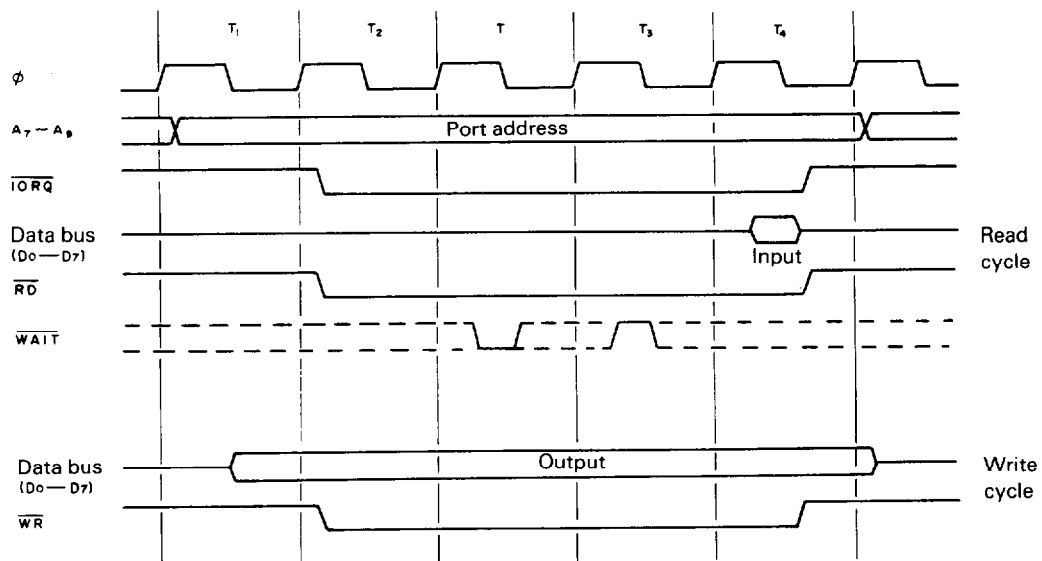


Fig. 7.9

3.4 Bus request/acknowledge cycle

Fig. 7.10 is the timing chart in the bus request/acknowledge cycle.

The CPU checks signal BUSRQ at the leading edge of the final clock pulse in each machine cycle. If signal BUSRQ is active, the CPU puts the address, data and tri-state control buses into HIGH impedance at the leading edge of the next clock pulse. From this time, these buses can be controlled by external units so that it is possible to use them in data transfer with memory and I/O unit. (This is commonly known as the cycle steal system direct memory access (DMA).)

The CPU response delay to the bus request is the length of one machine cycle at most. Thus, an external controller can control buses for the necessary time.

However, when it is necessary to continue DMA cycle for an extended period of time with dynamic memories, measures must be taken so that dynamic memories can be refreshed from an external controller. This case applies only when a number of data blocks are transferred in the DMA system. It should be noted that the interruption by signal NMI or INT is ignored in the state that use of buses is possible.

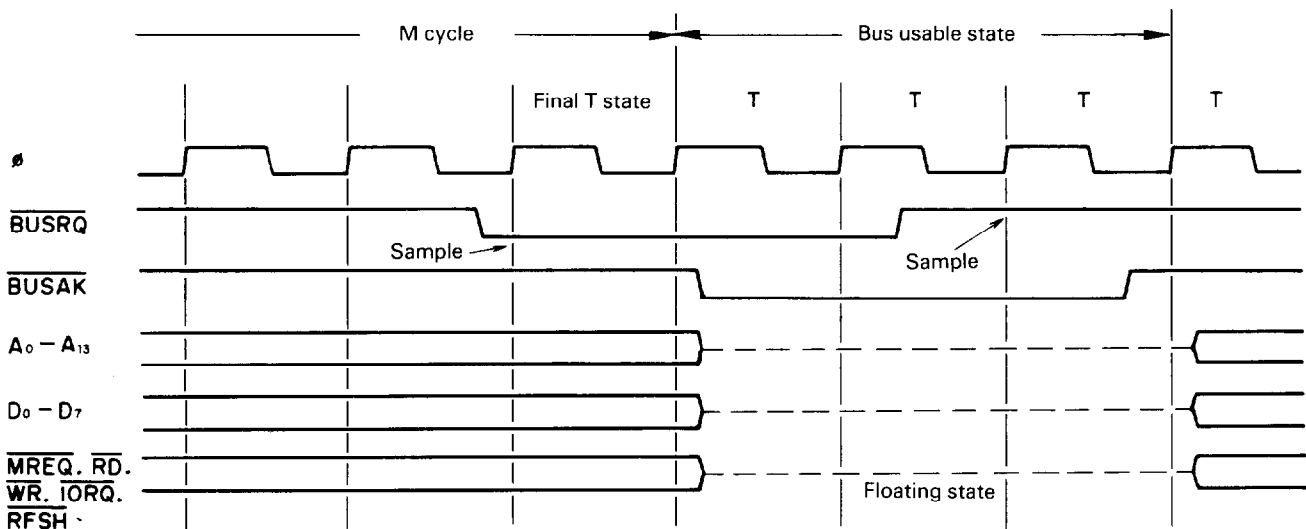


Fig. 7.10

3.5 Interrupt request/acknowledge cycle

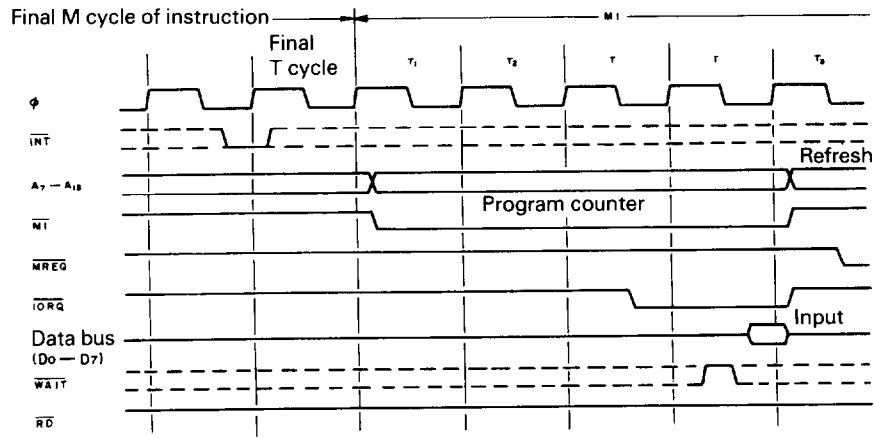
Fig. 7.11 is the timing chart relating to the interrupt request cycle.

The CPU samples interrupt request signal INT at the leading edge of the final clock pulse which is used for executing the instruction. This signal is not accepted unless the interrupt enable flip-flop is set within the CPU. The same also applies to the case that signal BUSRQ is active.

When this signal is accepted, the CPU generates a special M1 cycle.

During the period of this M1 cycle, signal IORQ becomes active in lieu of normal signal MREQ, thereby enabling an 8-bit vector to be put on the data bus from the unit which has issued the interrupt request. This is called "interrupt acknowledge". It should be noted that two cycles of wait state are added in the period of the M1 cycle.

Use of the ripple priority interrupt system becomes possible by addition of these cycles. If two cycles of wait state are given, the ripple signal is transmitted stably. Thus, the time sufficient to positively take in the I/O unit emitted response vector in the CPU is obtained.



* Wait state (signal pulse T_w) is inserted automatically.

Fig. 7.11

The method of prolonging the acknowledge time by use of a programmable counter is shown in Fig. 7.12 and 7.13.

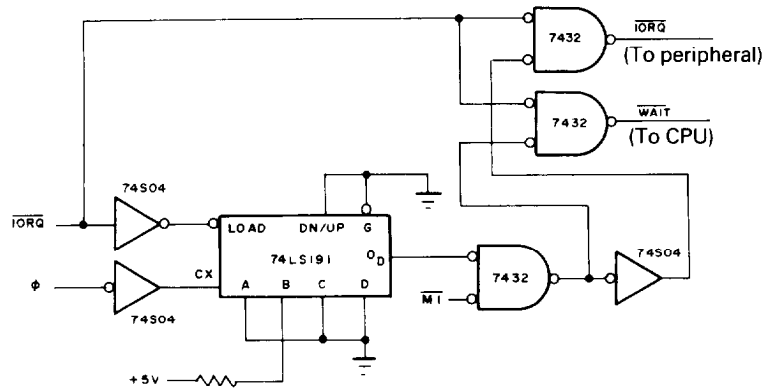


Fig. 7.12

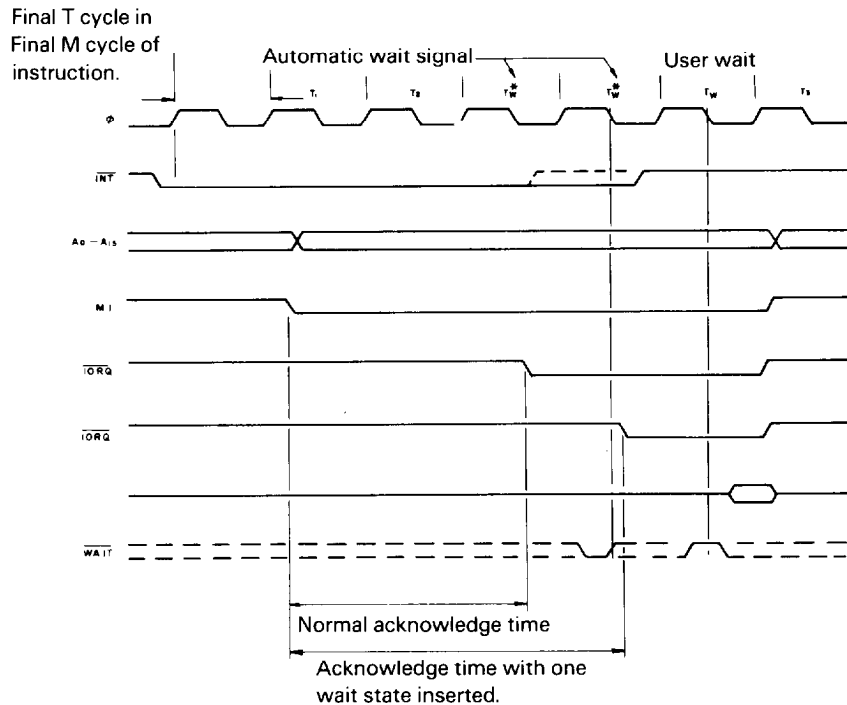


Fig. 7.13

3.6 Non-maskable interruption response

Fig. 7.14 is the timing chart in the non-maskable interrupt request/acknowledge cycle.

Differently from signal INT, signal NMI is effective at the trailing edge, and its input can be performed at any timing of the instruction. However, to enter the acknowledge cycle after the current instruction is completely executed, it is necessary to obtain the leading edge of signal NMI before the final T cycle of the instruction as a minimum requirement. This signal is higher in priority than signal INT and its function cannot be made invalid by the software.

The CPU responds the non-maskable interruption, just it would in the normal memory read operation. The difference in the CPU's response to the two signals is that the CPU automatically moves the contents of the program counter to an external stack when a non-maskable interrupt occurs regardless of the current contents of the data bus to jump to address 0066_H.

When this interruption system is to be used, it is needed to write the service routine for the non-maskable interruption from address 0066_H.

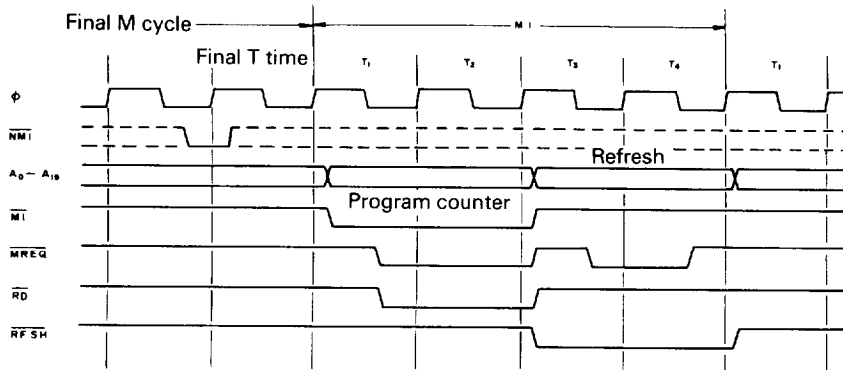


Fig. 7.14

3.7 Halt state clear

With command HALT of the program, the CPU continues executing command NOP. However, with an interrupt input, the CPU comes out of this state. (This case is applicable to the non-maskable interruption and the maskable interruption for which the interrupt flip-flop is set.)

As shown in Fig. 7.15 for these two interruptions, the CPU checks the interrupt request signal at the leading edge of each cycle of pulse T_4 and it is released from the halt state at the leading edge of the next clock pulse if this interruption is the case.

Next, the CPU enters the pertinent acknowledge cycle according to the type of the accepted interruption. If non-maskable and maskable interrupt request signals enter concurrently, the non-maskable interruption with higher priority is accepted.

In addition, command NOP is executed at the halt state for continuous emission of the memory refresh signal. In this state, the position in each T cycle is the same as in normal MI (fetch) cycle except that the data from the memory is ignored. Then, command NOP is executed automatically within the CPU. When command HALT is executed, signal HALT becomes active to indicate to external units that the CPU has entered the halt state.

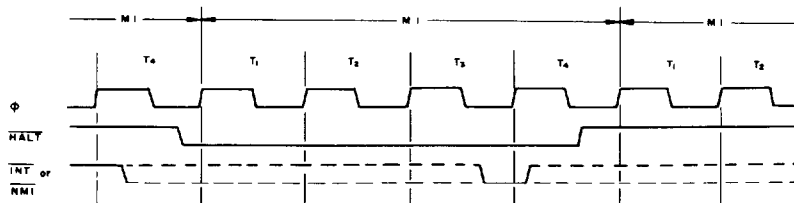
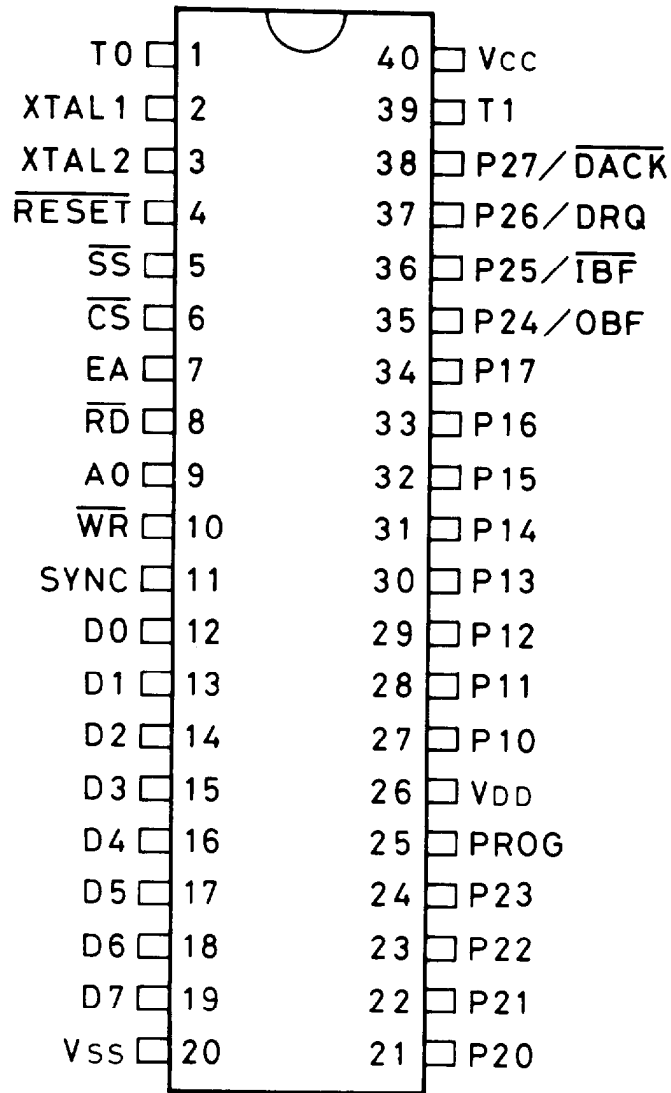


Fig. 7.15

(1) Terminal layout



8042/8741

Fig. 7.16 Pin configuration

(2) Block Diagram

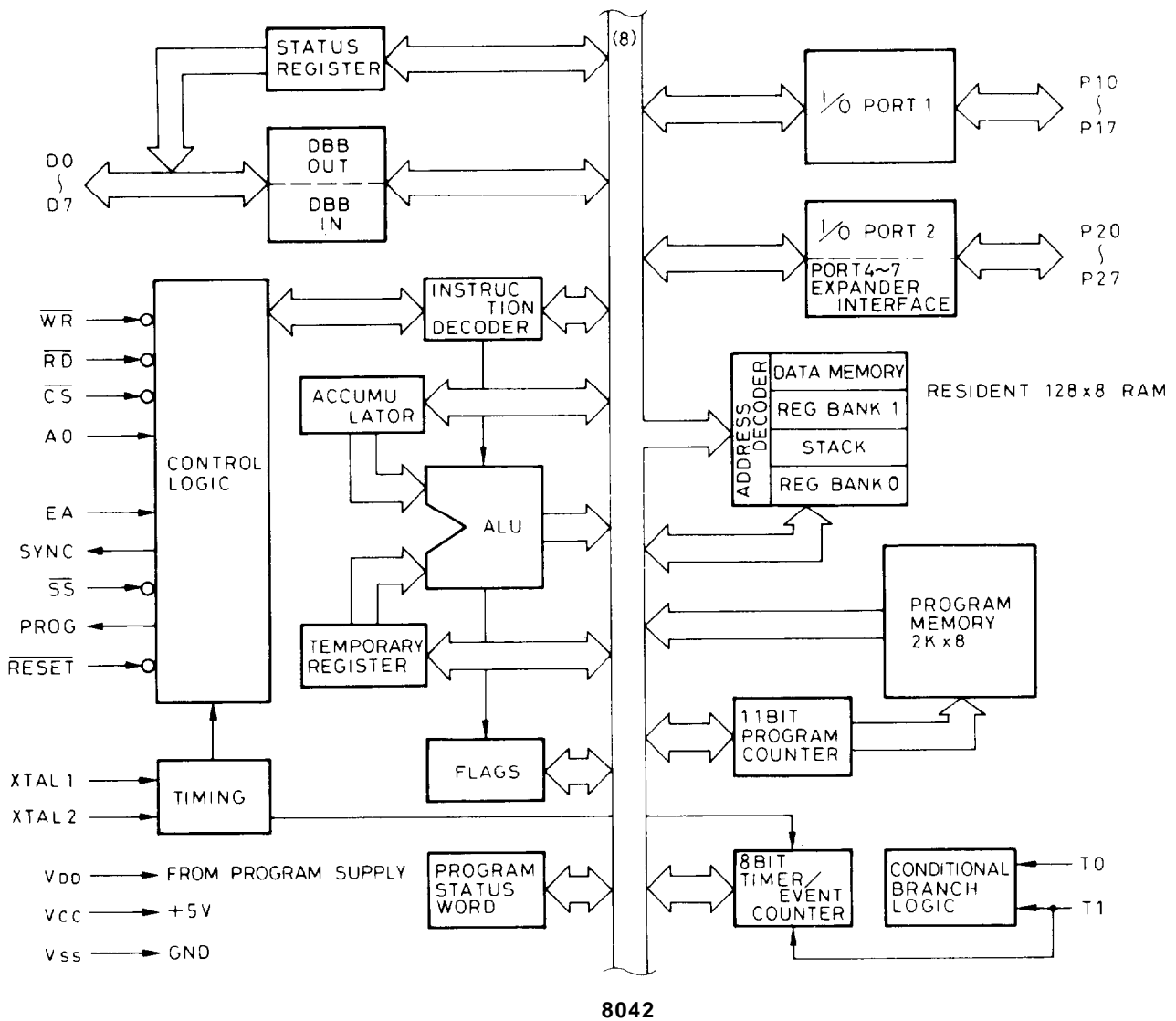


Fig. 7.17 Block diagram

(1) Features

- 8-bit microprocessor unit
- Built-in 2-kbyte ROM (1 K byte ROM)
- Built-in 128-byte RAM (64 byte RAM)
- 8-bit I/O port (2 sets)
- Two test input lines
- Built-in 11 -bit program counter (10 BIT)
- Built-in 8-bit timer/counter
- Built-in clock generator
- 8-bit status register
- Two data buffer registers
- 93 kinds of instructions
- DMA handshake interrupt request function

(2) Terminal functions of 8042/8742 (8041/8742)

- TO, T1 (Test Input 0, 1) Input
Input terminals for testing by conditional branch instruction.
T1 serves also for the event input of the event counter.
- XTAL 1, 2 (Crystal 1, 2)
Crystal connection terminals for built-in clock oscillation
- RESET...Input
- SS (Single Step).....Input
Terminal for control of single step operation. When signal is LOW, the MPU stops upon completion of the command being executed.
- CS (Chip Select).....Input
Chip select for selection of UPI.
- EA (External Access).....Input
Terminal for emulation and test of the UPI. At the input of “L” of “H” level in normal operation, the UPI enters the test mode.
- RD (Read Strobe).....Input
Strobe signal for the master processor to read out output data buffer register or status register.
- A0 (Address O).....Input
A0 = “L”: Read-out of data from output data bus buffer register or write-in of data to input bus buffer register
A0 = “H”: Read-out from status register or write-in of command to input data bus buffer register
- WR (Write Strobe).....Input
Strobe signal for the master processor to write data or command in input data bus buffer register
- SYNC (Synchronism)
Signal output for an instruction cycle. SYNC output is used as a strobe signal to external circuits. It is also used to synchronize single stpe operation.
- DO to D7 (Data).....Input/Output
8-bit bidirectional data bus.
The data bus is in high impedance, except when the master processor is reading out the UPI.

● P20 to P27 (I/O port 2).....Input/Output

In addition to the ordinary functions of the I/O ports, there are the following functions:

The lower four bits (P20 to P23) can also serve as the interface ports with the uPD8243 I/O expander. When the expanded I/O ports (Ports 4 to 7) are accessed, the address, command and data are transmitted. At single step operation, the higher three bits of program fetch address are output to P22 and P20.

By software control, the following higher four bits (P24 to P27) can be used as the terminals for interrupt request and DMA (Direct Memory Access) handshake:

P24: OBF (Output Data Bus Buffer Register Fu 11) output terminal

P25: IBF (Input Data Bus Buffer Register Ful 1) output terminal

P26: DRQ (DMA Request) output terminal

P27: DACK (DMA Acknowledge) input terminal

● PROG (Program).....Input/Output

Strobe signal to the 8243 I/O expander.

This terminal serves as the input terminal of program pulse at write to the ROM inside the 8742 (with built-in EPROM).

● VDD

+5V power source for the built-in RAM

● P10 to P17 (I/O Port 1).....Input/Output

8-bit bidirectional I/O port.

At single step operation, these terminals serve as the output terminals for the lower 8 bits of program fetch address.

● T1 (Test 1)

● VCC (+5V Power Supply Terminal)

(5) Timing diagram

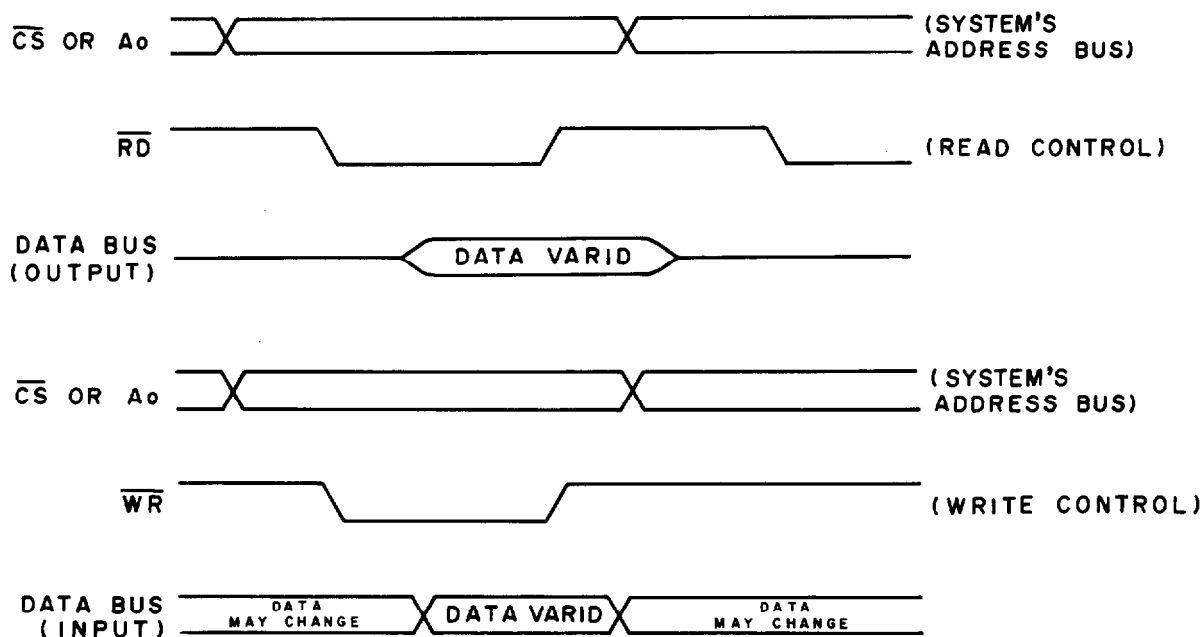


Fig. 7.18

Programmable interrupt controller uPD8259AC

- 8-level priority controller
- Extendible up to 64 levels
- Interrupt mode programmable
- Individual reuest mask
- CALL command code generation
- N-channel MOS
- I/O, TTL compatible
- Single power supply, +5V
- 28-pin plastic DIP (D-28C)

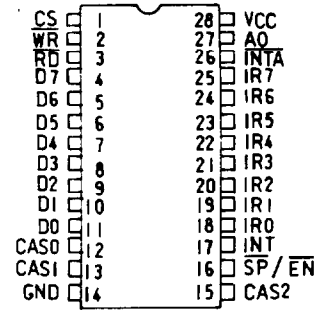


Fig. 7.19

Names and functions of pins

CS: Chip select

WR: Write input

RD: Read input

D₇ - D₀: Data bus

CAS0 - CAS2:

When used as master (SP = 1), they become outputs, while when used as slave (SP = 0), they become inputs. CAS lines form individual 8259A buses to control the system using a plural number of 8259A units.

SP/EN:

Slave program input/enable output

This pin has two functions. In buffer mode, it works as the output pin (EN) to enable the buffer transceiver. In non-buffer mode, it works as the input pin (SP) to determine whether 8259A acts as master (SP = 1) or slave (SP = 0).

INTA:

Interrupt acknowledge input

Used to enable the interrupt vector data in 8259A to be output on the data bus.

This process is generated from the CPU side.

INT:

Interrupt request output

IRO - IR7:

Interrupt request input

AO:

Command select address

uPD8259A controls priority provided interruptions of up to 8 levels. It can be extended up to 64 levels.

Programmable peripheral interface uPD8255AC-5

- Compatible with uPD8085A microprocessor
- Controllable directly from CPU for setting and resetting each bit.
- TTL compatible
- 40-pin plastic DIP (D-40C)
- Compatible with Intel 8255A-5
- 4 MHz operation
- Power supply, $V_{cc} = +5V \pm 10\%$

PA3	1	40	PA 4
PA2	2	39	PA 5
PA1	3	38	PA 6
PA0	4	37	PA 7
\overline{RD}	5	36	\overline{WR}
\overline{CS}	6	35	RESET
GND	7	34	D0
A1	8	33	D1
A0	9	32	D2
PC7	10	31	D3
PC6	11	30	D4
PC5	12	29	D5
PC4	13	28	D6
PC0	14	27	D7
PC1	15	26	VCC
PC2	16	25	PB7
PC3	17	24	PB6
PB0	18	23	PB5
PB1	19	22	PB4
PB2	20	21	PB3

Names and functions of pins

$D_0 - D_7$:	Data bus (two-way)
\overline{CS} :	Chip select
RESET:	Reset
\overline{RD} :	Read control
\overline{WR} :	Write control
A_0, A_1 :	Port address
$PA_0 - PA_7$:	Port A I/O
$PB_0 - PB_7$:	Port B I/O
$PC_0 - PC_7$:	Port C I/O

Fig. 7.20 Pin configuration

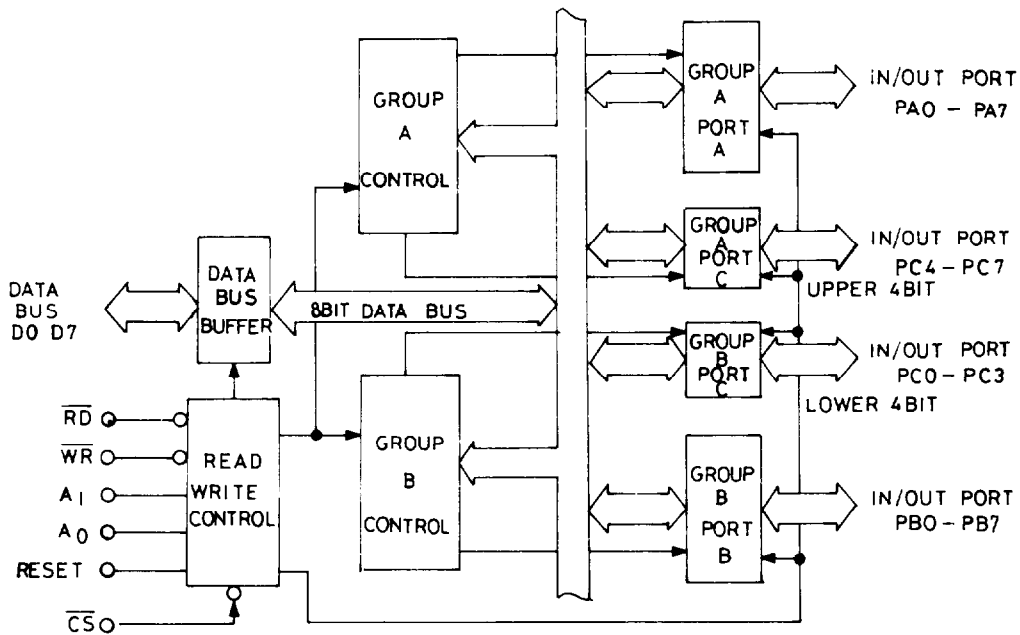
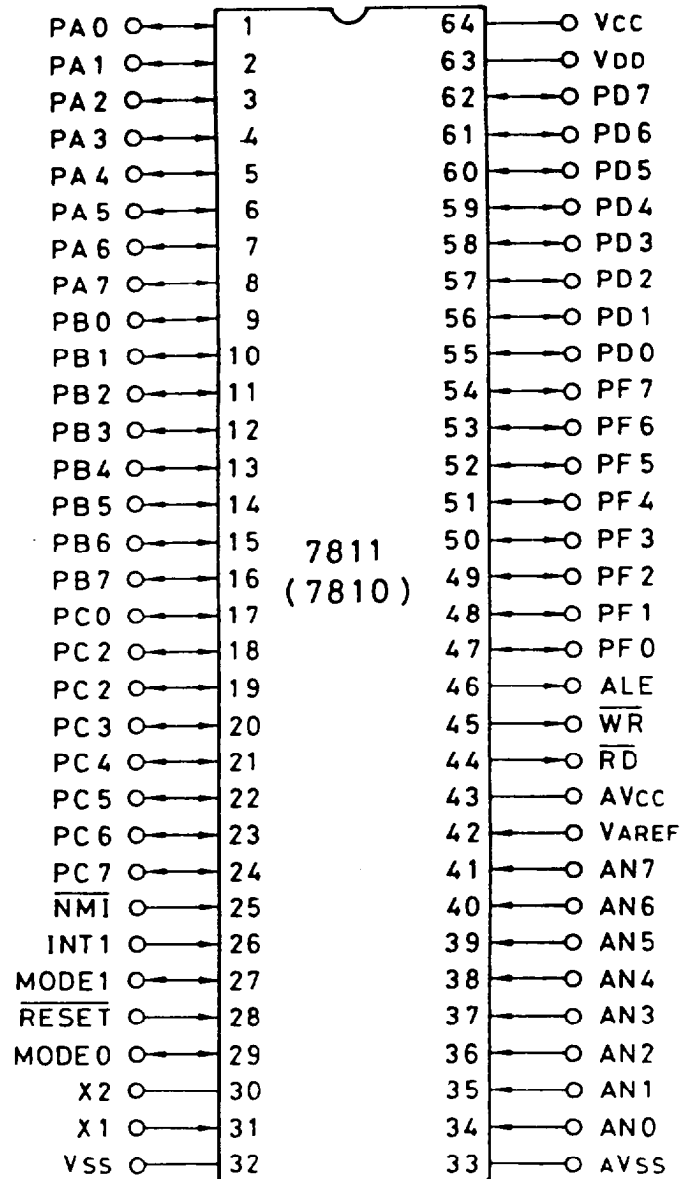


Fig. 7.21 Block diagram

uPD8255A-5 is a programmable general-purpose I/O unit developed for the pPD8085A microprocessor system. The unit, with 3 sets of I/O ports (8-bit), is available for data input, data output, status signal input and control signal output on program control.

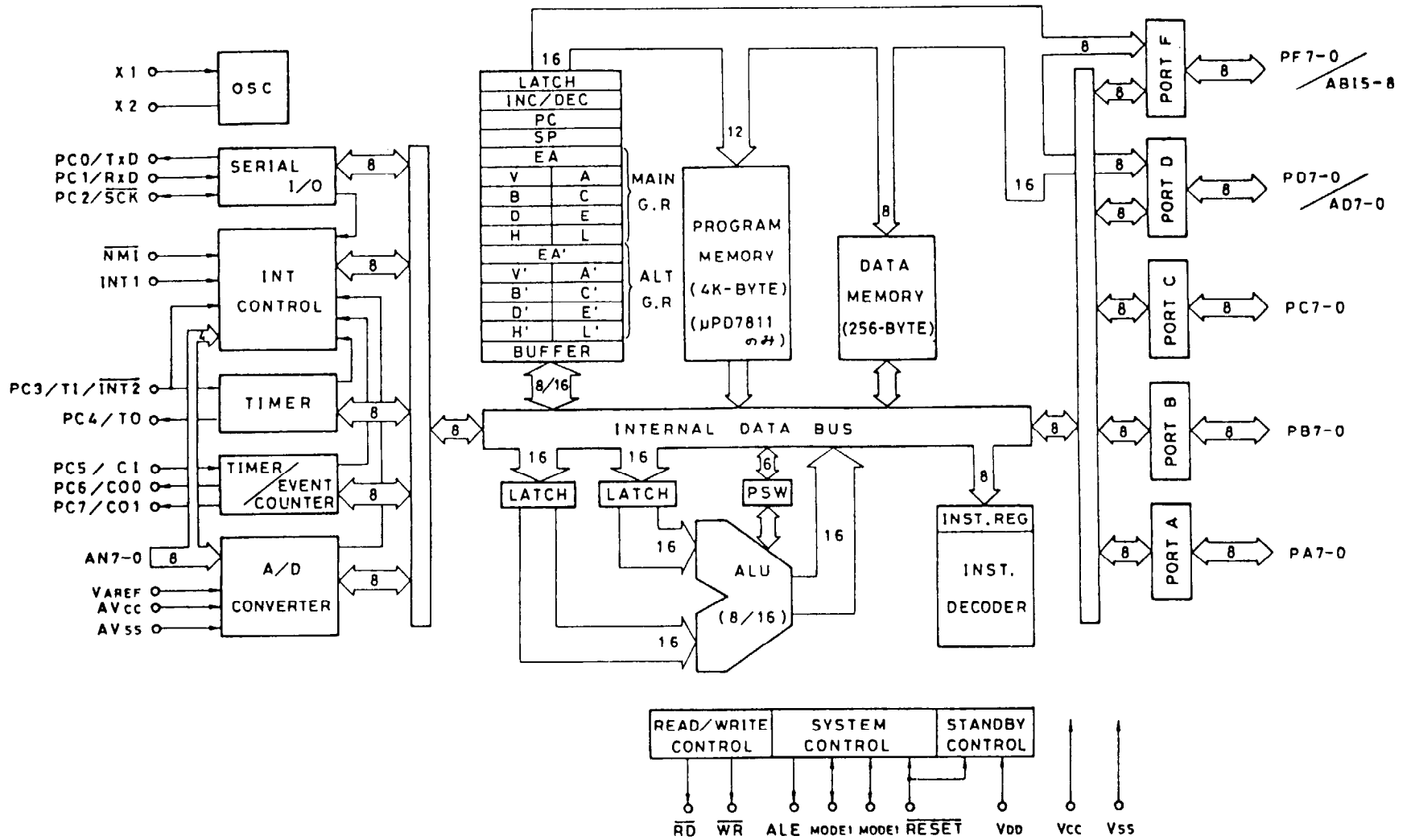


Pin configuration

- | | | | |
|-------|--------------------------|--------------|------------------------|
| PA7-0 | : Port A | MODE0.1 | : Mode0.1 |
| PB7-0 | : Port B | x1,x2 | : Crystal |
| PC7-0 | : Port C | AN7-0 | : Analog Input |
| PD7-0 | : Port D | RD | : Read Strobe |
| PE7-0 | : Port F | WR | : Write Strobe |
| NMI | : Non-maskable Interrupt | ALE | : Address Latch Enable |
| INT1 | : Interrupt Request | <u>RESET</u> | : Reset |
| | | VAREF | : Reference Voltage |

Fig. 7.22 Pin Configuration

Fig. 7.23 Block Diagram



Operation of 7811 Port F

Table 7.3

PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0	External Memory
Port	Port	Port	Port	Port	Port	Port	Port	256 bytes (max.)
Port	Port	Port	Port	AB11	AB10	AB9	AB8	4K bytes (max.)
Port	Port	AB13	AB12	AB11	AB10	AB9	AB8	16K bytes (max.)
AB15	AB14	AB13	AB12	AB11	AB10	AB9	AB8	60K bytes (max.)

● **7810**

(a) By setting modes 0 and 1, assignment to the address bus (AB15 to 8) can be made in accordance with the size of memory to be provided externally.

The remaining terminals can be used as input/output ports.

See the following table.

Operation of 7810 Port F

Table 7.4

MODE1	MODE0	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0	External Memory
0	0	Port	Port	Port	Port	AB11	AB10	AB9	AB8	4K bytes
9	1	Port	Port	AB13	AB12	AB11	AB10	AB9	AB8	16K bytes
1	1	AB15	AB14	AB13	AB12	AB11	AB10	AB9	AB8	64K bytes

6) **WR (Write Strobe).....Output**

Strobe signal for write operation of external memory.

HIGH level at times other than the data write machine cycle of external memory and at reset.

7) **RD (Read Strobe).....Output**

Strobe signal for read operation of external memory.

HIGH level at times other than the read machine cycle of external memory and at reset.

8) **ALE (Address Latch Enable).....Output**

Strobe signal to latch the lower 8 bits of address to access external memory.

9) **MODE 0, MODE 1 (Mode).....Input/Output**

● 781 1: Mode 0 is set at LOW level and Mode 1 at HIGH level.

● 7810: Mode 0 and Mode 1 are set in accordance with the size of external memory.

Table 7.5

Mode	Mode 0	External memory
0	0	4KB Addresses 0 to 0FFF
0	1 (Note)	16KB Addresses 0 to 3FFF
1 (Note)	1 (Note)	64KB Addresses 0 to FEFF

(Note) pull-up is made

Functions of Mode 0 and Mode 1

The following two functions are made possible by pulling up the Mode terminal:

(1) Mode 0: Output of 10/M in synchronism with ALE

(2) Mode 1: Output of MI in synchronism with ALE

- 10) NMI (Non-maskable Interrupt).....Input
Non-maskable interrupt of the edge trigger (trailing edge)
- 11) INTI (Interrupt).....Input
Maskable interrupt input of the edge trigger (leading edge). It can also be used as the AC input zero cross detecting terminal.
- 12) AN7-0 (Analog Input).....Input
8 analog inputs of A/D converter. And AN7 to 4 can be used as the input terminals to detect the leading edge and to set the test flag upon detection of the trailing edge.
- 13) VAREF (Reference Voltage).....Input
Reference voltage input of the A/D converter
- 14) AVcc (Analog VCC)
Power terminal of the A/D converter
- 15) AVss (Analog Vss)
GND terminal of the A/D converter
- 16) VDD
Power supply to the built-in RAM which supplies +5V during normal operation and Standby.
- 17) XI, X2 (Crystal)
Crystal connection terminal for built-in clock pulse. When the clock pulse is supplied from outside, input must be made to XI.
- 18) $\overline{\text{RESET}}$ (Reset)
Reset input at LOW level
At the reset input, the conditions of respective ports are as follows:
- | | |
|---------------|---|
| Port A: | Input port (Output high impedance) |
| Port B: | Input port (Output high impedance) |
| Port C: | Input port (Output high impedance) |
| Port D | |
| (a) uPD7811: | Input port (Output high impedance) |
| (b) ,uPD7810: | Address output at PD7 to 0 |
| Port F | |
| (a) uPD7811: | Input port (Output high impedance) |
| (b) uPD7810: | Terminal designated by address bus is for address output.
Port terminal becomes an input port. |

Timing (See page 7-26)

- 3 cycles of oscillation frequency are defined to be one state.
- One machine cycle requires 3 states for read or write operation, and OP code fetch requires 4 states.
- Wait state cannot be inserted.

(1) OP code fetch timing

Four states (T1 - T2) constitute the OP code fetch timing. During T1 to T3 program memory is read; instructions are interpreted during T4.

AB15 to 8 (PF 7 to 0) are output to T1 - T4.

AD7 to 0 (PD7 to 0) are used in the multiplex mode; in this mode, the address is latched during T1 at the ALE signal. Since the memory addressed is enabled after discharging the driver, AD7 to 0, RD signal output to T1 to T3, fetched at T3 and processed internally at T4.

(2) Memory read

Memory read is performed during T1 to T4.

ALE and RD signals are executed from T1 to T3; OP code fetch for these two signals is performed at T4.

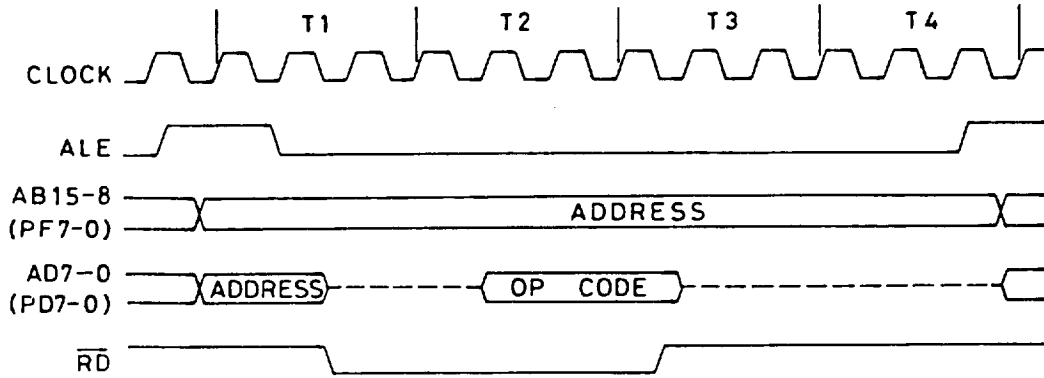
(3) Memory timing

Memory write is performed during T1 to T3.

The Address and ALE signal timing is the same as for memory read. However, following address output, AD7 to 0 (PD7 to 0) are not disabled, and write data are output at AD7 to 0 from the beginig of T1 to the end of T3.

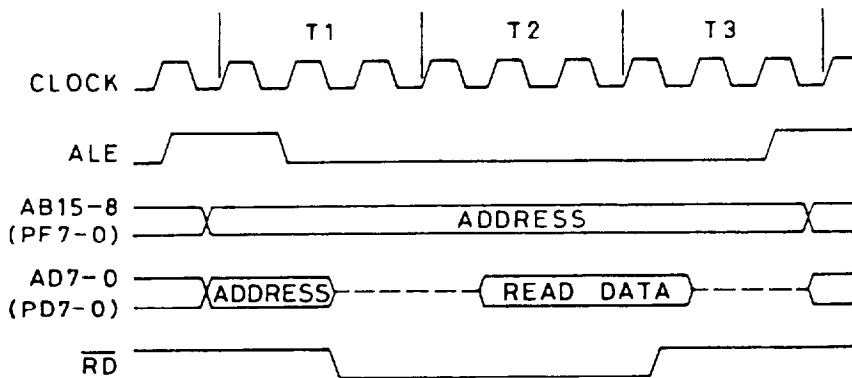
The WR signal is output from the middle of T1 to the start of T3.

Note: Where PD7 to 0 are set to the multiplex address/data bus (AD7 to 0) and PF7 to 0 to the address bus (AB15 to 7), the RD and WR signals in the machine cycle not accessing external memory are both at HIGH level.



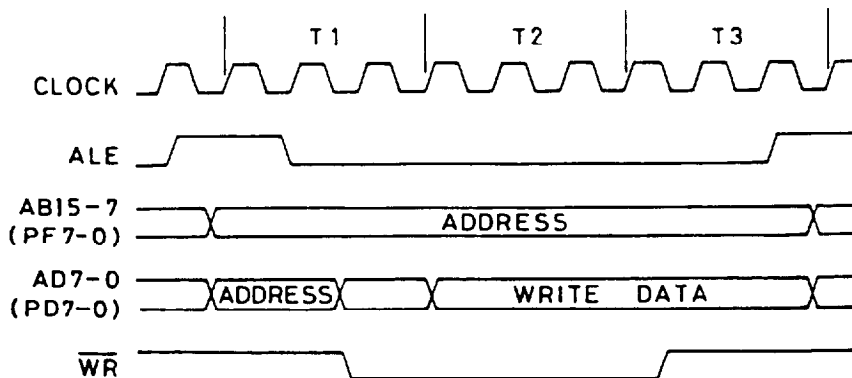
O? Code Fetch Timing

Fig. 7.24



Memory Read Timing

Fig. 7.25



Memory Read Timing Oscillation

Fig. 7.26

Gate array uPB6101-009

- Receiving signal I/F of Z-80 or Z-80A CPU, or Intel type peripheral LSI (8041 A, 8255A, 8259A, etc.) and controlling drum.
- Operable at about 4 MHz with one wait state inserted to Z-80A CPU in OP code fetch only, and at about 2.5 MHz without no wait state.
- 28-pin DIP

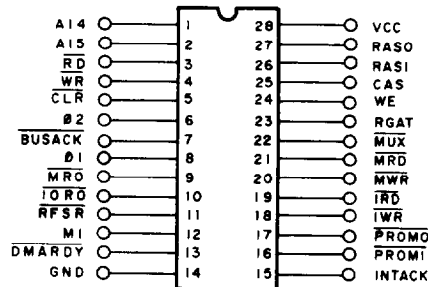


Fig. 7.27

Names and functions of pins

CLR (input):	Clear Initializes IC at LOW.
Ø0, Ø1 (input):	2-phase clock signal Ø ₁ is in anti-phase with clock pulse of Z-80 CPU.
A15 (input):	MS8 on address bus
A14 (input):	No. 14 bit on address bus
MRQ (input):	Memory request
IORQ (input):	I/O request
RFSH (input):	Refresh
MI (input):	Machine cycle 1
RD (input):	Read strobe
WR (input):	Write strobe
BUSACK (input):	Bus acknowledge
DMARDY (I/O):	DMA ready
	When accessing drum, outputs LOW pulse automatically to apply one cycle of wait state.
INTACK (output):	Interrupt acknowledge
PROM0, PROM1 (output):	Program select 0, 1
	Connected to chip enable pin of ROM where program is. When they are LOW, program ROM chip is enabled.
RAS0, RAS1 (output):	Row address select 0, 1
	When they are HIGH, row address select signal is sent to drum through inverter.
CAS (output):	Column address select
	When this signal is HIGH, column address select signal is sent to drum through inverter.
MUX (output):	Multiplexer
	Drum address multiplexer select signal
WE (output):	Write enable
	This signal is sent via inverter for writing on drum.
RGAT (output):	Drum data bus output enable signal
IWR (I/O):	I/O write signal
IRD (I/O):	I/O read signal
MRD (I/O):	Memory read signal
MWR (I/O):	Memory write signal

Programmable interval timer 8253-5

- 3 independent 16-bit counters
- From DC to 2 MHz
- Programmable count mode
- Binary or BCD count
- Single power supply, +5V
- 24-pin DIP
- I/O, TTL compatible
- Compatible with 8085A

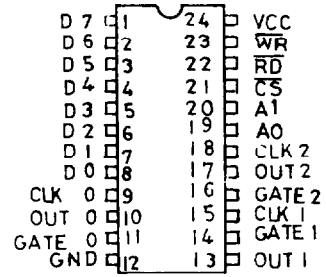


Fig. 7.28

Names and functions of pins

- Do-D7:** Data bus (8-bit)
- CLK N:** Counter clock pulse input (N = 0 - 2)
- GATA N:** Counter gate input (N = 0 - 2)
- OUT N:** Counter output (N = 0 - 2)
- RD:** Read counter
- WR:** Write command/data
- cs:** Chip select
- Ao, Ai :** Counter select 0, 1

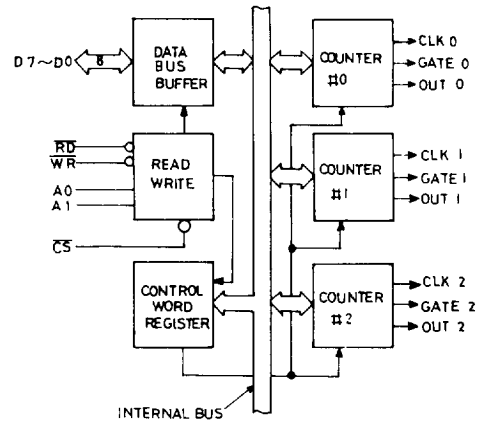


Fig. 7.29

Precision timer NE555

- Timing generation of from usec to hour
- I/O, TTL compatible
- Duty cycle adjustable

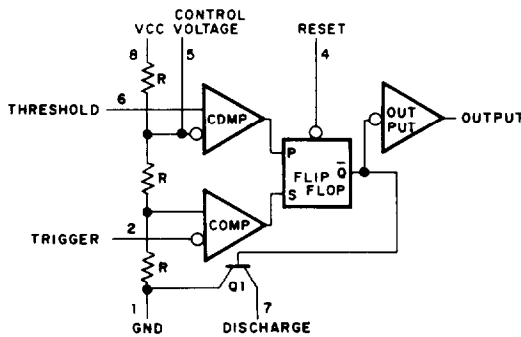


Fig. 7.31

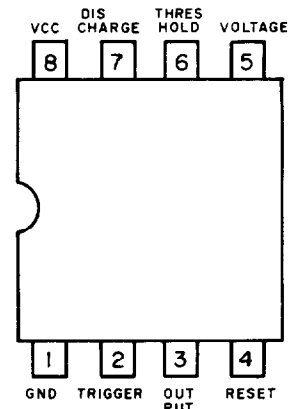


Fig. 7.30

Names and functions of pins

- DISCHARGE:** Discharge
Discharge path of external capacitor when flip-flop becomes HIGH with trigger
- THRESHOLD:** Threshold
 $2 / 3 V_{cc}$
- CONTROL VOLTAGE:** Control voltage
Threshold and trigger voltage level control pin
- TRIGGER:** Trigger
 $1/3 v_{cc}$
- OUTPUT:** output
Timer output pin
- RESET:** Reset

When the trigger input becomes lower than the trigger level, the flip-flop is set so that its output becomes HIGH.

When the threshold input becomes higher than the threshold level, the flip-flop is reset so that its output becomes LOW.

When the reset input becomes LOW, the flip-flop is reset so that its output becomes LOW.

When the output becomes LOW, the impedance between the discharge pin and GND is made LOW.

Loads of up to 200 mA can be connected to the output pin.

Dual differential comparator LM2903

- Usable with single power supply
- Supply voltage at wide range of 2 - 36V
- Operable at small current, 0.5 mA typical
- Small input bias and offset parameter
 - Input offset voltage, 2 mV typical
 - Input offset current, 5 nA typical
 - Input bias current, -25 nA typical

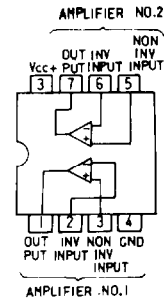


Fig. 7.32

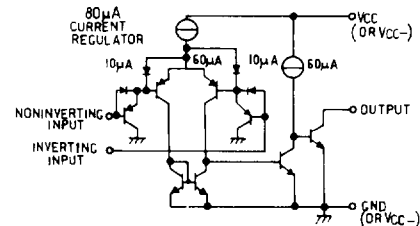


Fig. 7.33

4-bit two-way bus driver uPB8216C/D

- HIGH output voltage, $V_{OH} (DO) = 3..65V$ min
- Buffer configuration with small input current ($I_{II} = 0.25$ mA max.) and high output drive capability ($I_{OL} (DB) = 55$ mA max.)
- System configuration around CPU, simplified
- Compatible with Intel 8216
- 16-pin plastic DIP (8216C (D-I 6C)), 16-pin ceramic DIP (8216D (D-I 6D-S))

Names and functions of pins

- DB0 - DB3: Data bus
- DI0 - DI3: Data input
- DO0 - DO3: Data output
- DIEN: Data-in enable
- CS: Chip select

DIEN	CS	FUNCTION
0	0	DI - DB
1	0	DB - DO
0	1	High Impedance
1	1	

Table 7.6

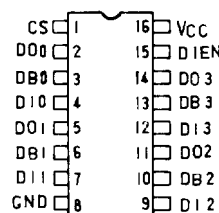


Fig. 7.34

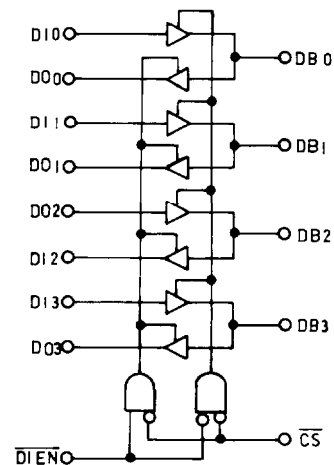


Fig. 7.35

I/O extension port 8243

- I/O port
 - 4 sets x 4-bit I/O ports
 - 1 set x 4-bit I/O ports
- AND/OR logic operation output
- N-channel MOS
- Single power supply, +5V
- 24-pin plastic DIP (D-24C)

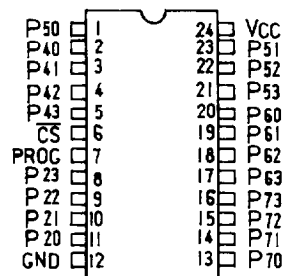


Fig. 7.36

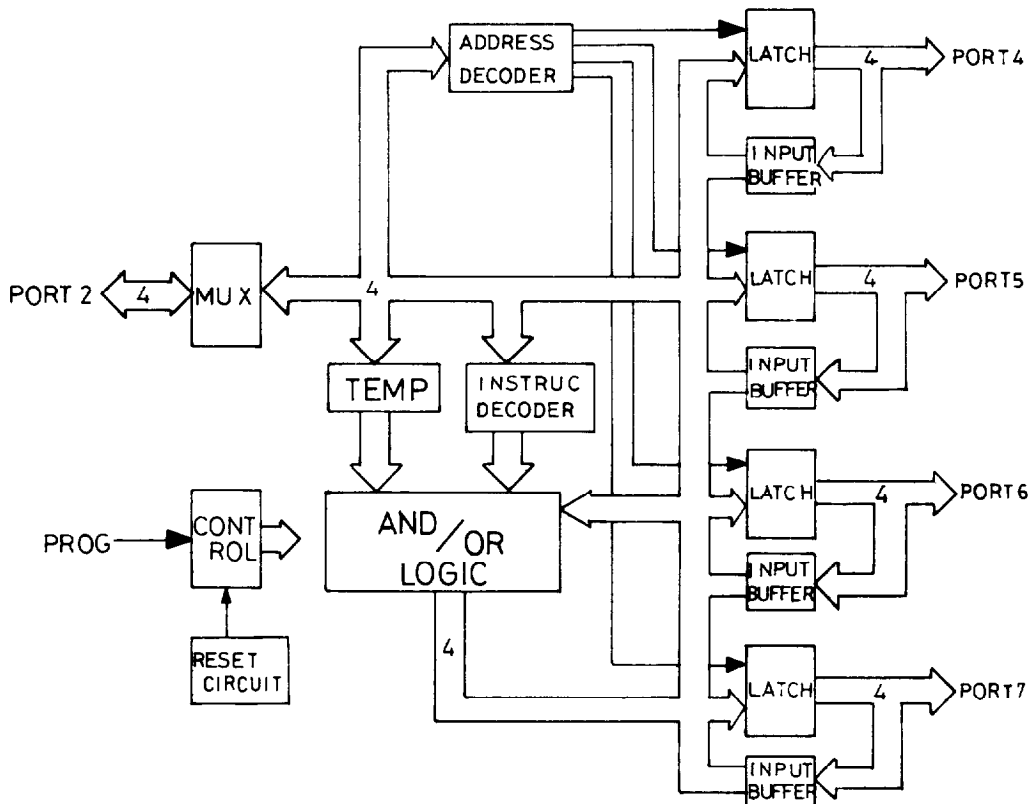


Fig. 7.37

Names and functions of pins

P20 - P23:	Port 2
P40 - P43:	Port 4
P50 - P53:	Port 5
P60 - P63:	Port 6
P70 - P73:	Port 7
CS:	Chip select
PROG:	Program pulse

The clock pulse used to obtain the timing of data output to CPU, or data or command input from CPU, is entered to this pin.

8243 takes in the command emitted to port 2 from CPU at the trailing edge of this pulse and, at the leading edge, controls the data designated by the command.

128K (16Kx8) EPROM 27128

- 16,324W x 8 configuration
- Access time, 250 ns max.
- Low-power standby mode
- I/O, TTL compatible
- N-channel MOS
- Single power supply, +5V
- 28-pin ceramic DIP

Names and functions of pins

A ₀ -A ₁₃ :	Address
CE:	Chip enable
OE:	Output enable
00-07:	output
PGM:	Program

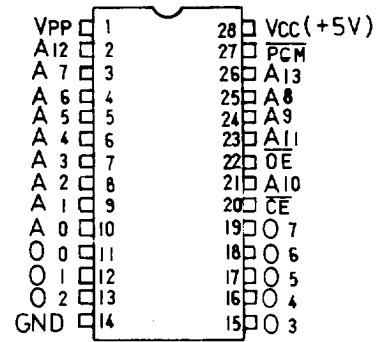


Fig. 7.38

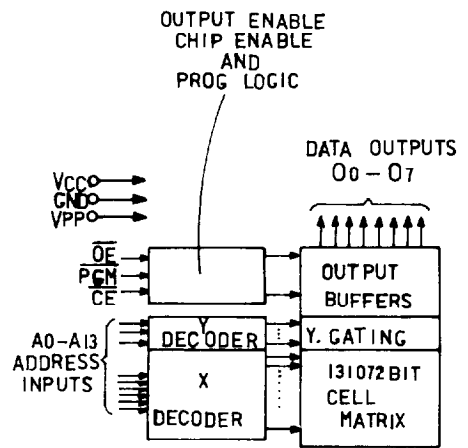
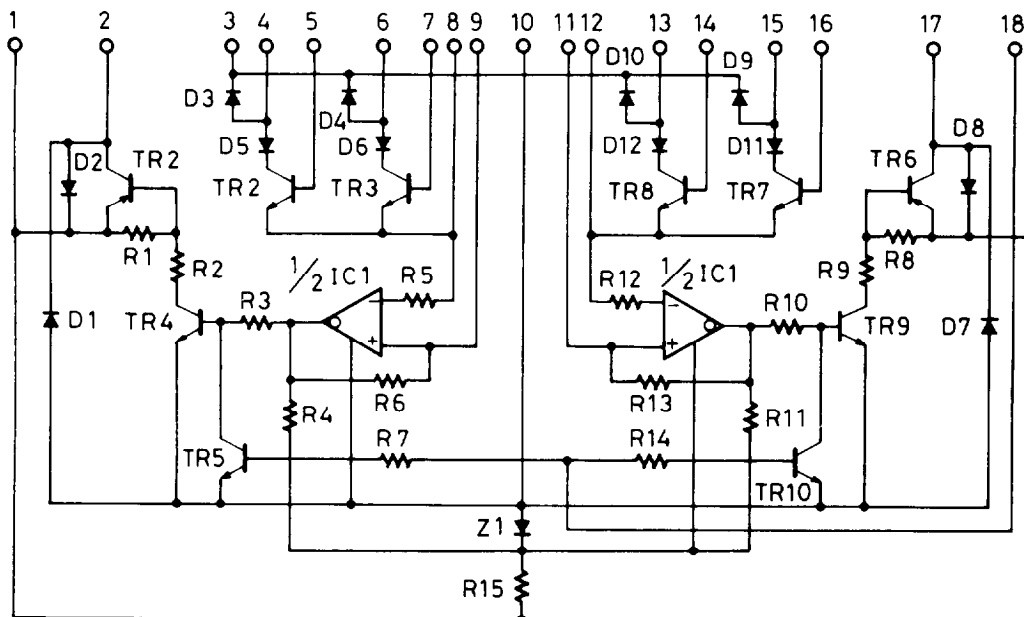


Fig. 7.39

Thick film IC STK6982

Names and functions of pins

Vp:	Power supply
CAB :	Common AB, common power supply line
Ccd:	Common CD, common power supply line
COM:	Common
	With Zener diodes connected to this pin, the voltages at pins On - Od can be clamped.
IA - ID:	Input pins to which signals are entered to turn ON or OFF transistors TR2, TR3, TR7 and TR8 with TTL level.
OA - OD:	Load connection pins
	Loads are connected between these and pin CAB or Ccd.
EAB, ECD:	Pins with logic signal ground level
s12, s34:	Pins with reference voltage
	With this level of reference voltage, it is possible to restrict the amount of power supplied to loads.
HOLD:	Control signal input pins to hold transistors TR4 and TR9
	When this pin is made "H", TR5 and TR11 turn ON. Thus, TR4 and TR9 turn OFF since their bases become "L". TR2 and TR6 thereby turn OFF so that no power (Vp) is supplied to loads.



STK6982

Fig. 7.40

Quad driver HA1 3007

- Dielectric strength 50V, max. output current 0.7 A
- Low saturation voltage between collector and emitter
- Input, TTL compatible
- Surge absorption diode against inductive load incorporated
- Small input current

Names and functions of pins

OUT A - OUT D: output

INA-IND: Input

ENABLE: Enable

When this pin is HIGH, this chip (HA1 3007) becomes effective.

CLAMP: Clamp

With Zener diodes connected to this pin, the voltages at OUT A - OUT D can be clamped.

HA1 3007 is a monolithic bipolar type, high-voltage, large-current quad driver, suitable for interface with high voltage or large current as in peripheral equipment, relay, solenoid, stepping motor, etc., including low-level logic operation.

ENABLE	IN	OUT
H	H	L
H	L	H
L	X	H

for each input:

H = High level; 2.0V

L = Low level; 0.8V

K = Irrelevant

Table 7.7

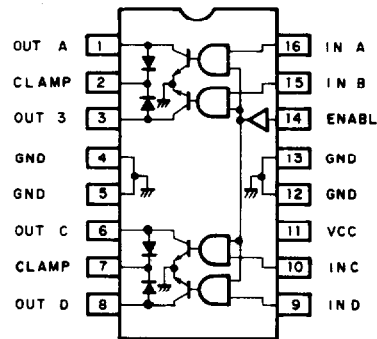


Fig. 7.41

Silicon transistor array μ PA79C

- Low output saturation voltage
- High DC current amplification factor
- Reverse bias protection diode incorporated in input side
- Surge absorption diode incorporated in output side

I : Input (Base)
 O : Output (Collector)
 GND : Common (Emitter)
 Vcc : Supply Voltage

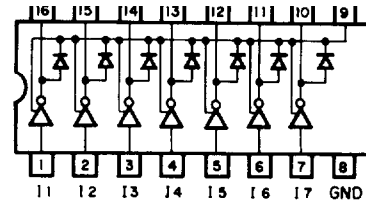


Fig. 7.42

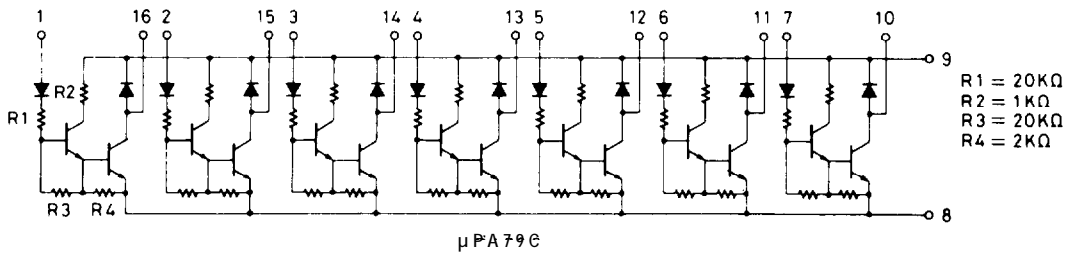


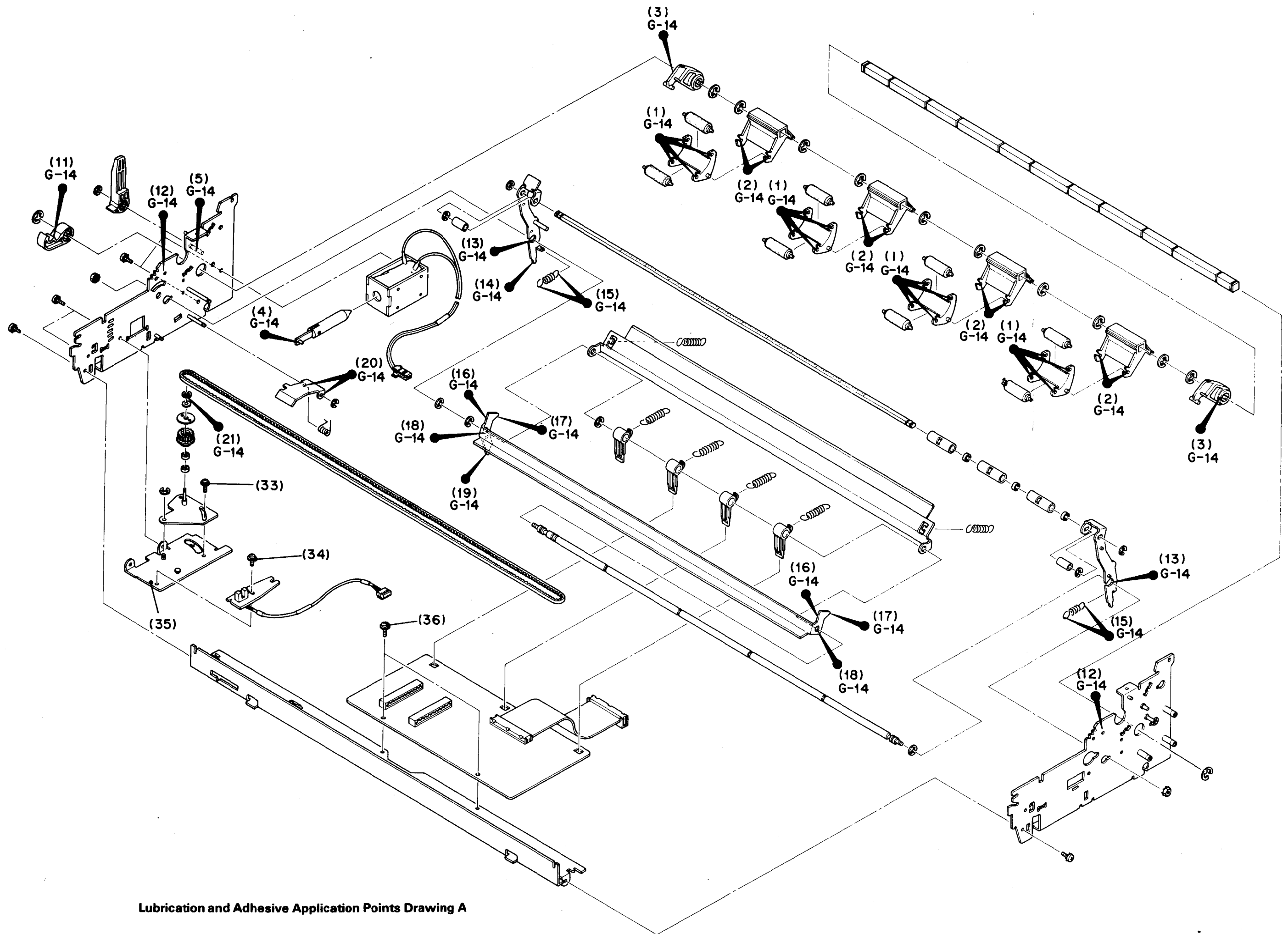
Fig. 7.43 μ PA79C

μ PA79C is a transistor array in which a 7-circuit configuration with NPN silicon transistors, diodes and peripheral resistors is made into a monolithic IC.

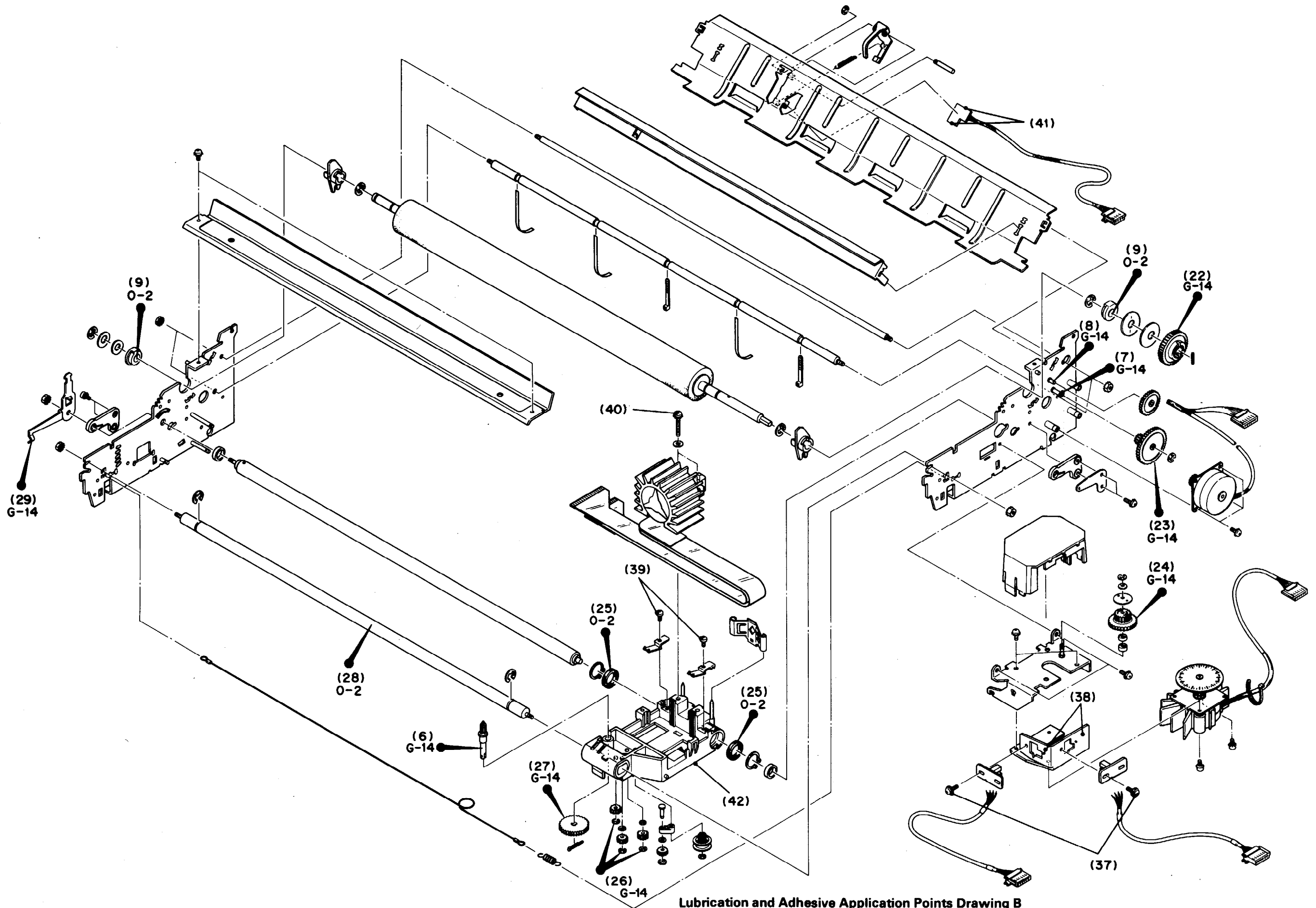
As this device, with low output saturation voltage, can drive about 100 mA load with MOS IC output signal, it is most suitable for the low-voltage drive type printer driver.

Names and functions of pins

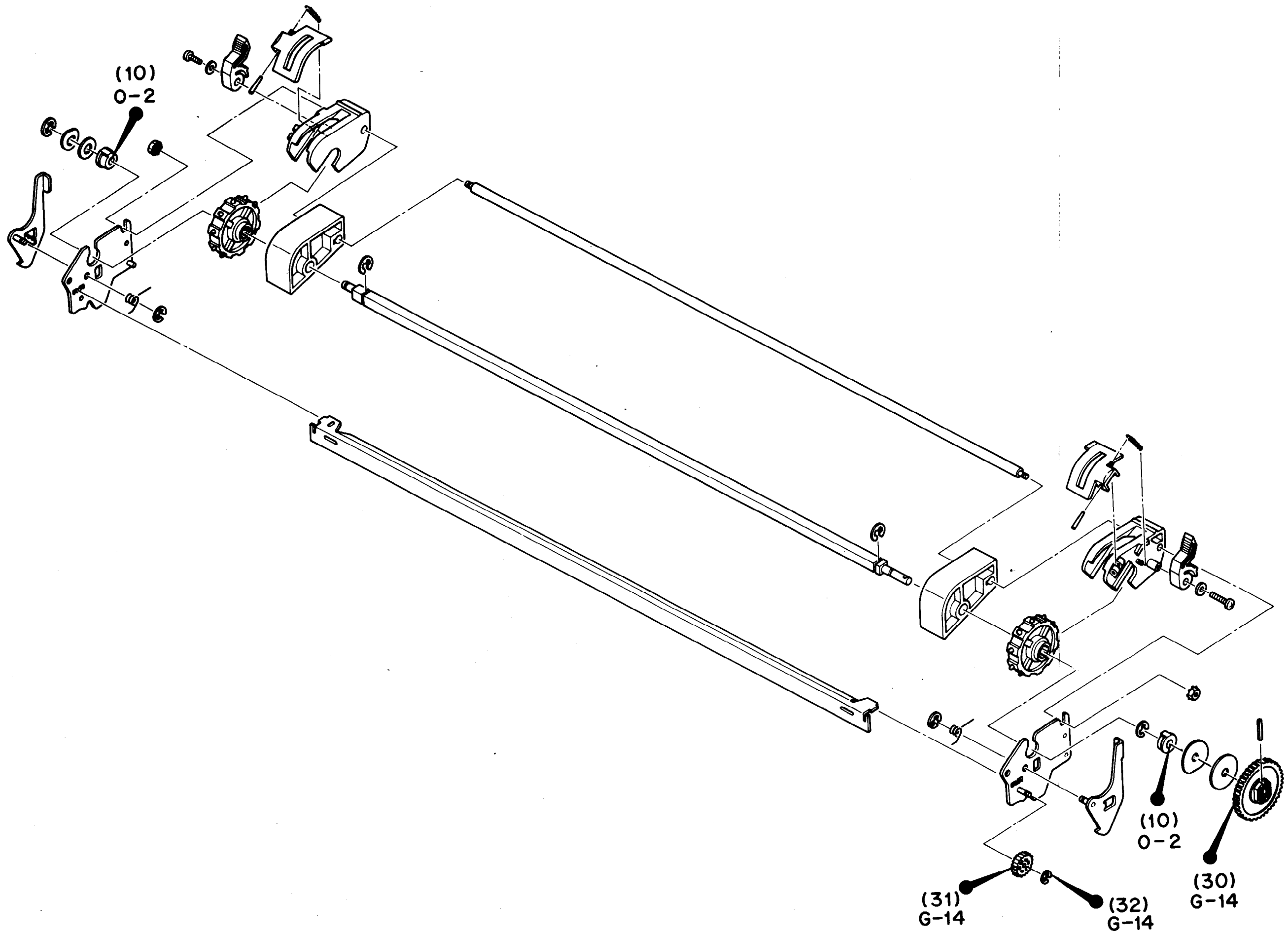
11 - 17: Input pins
 01 - 07: Output pins



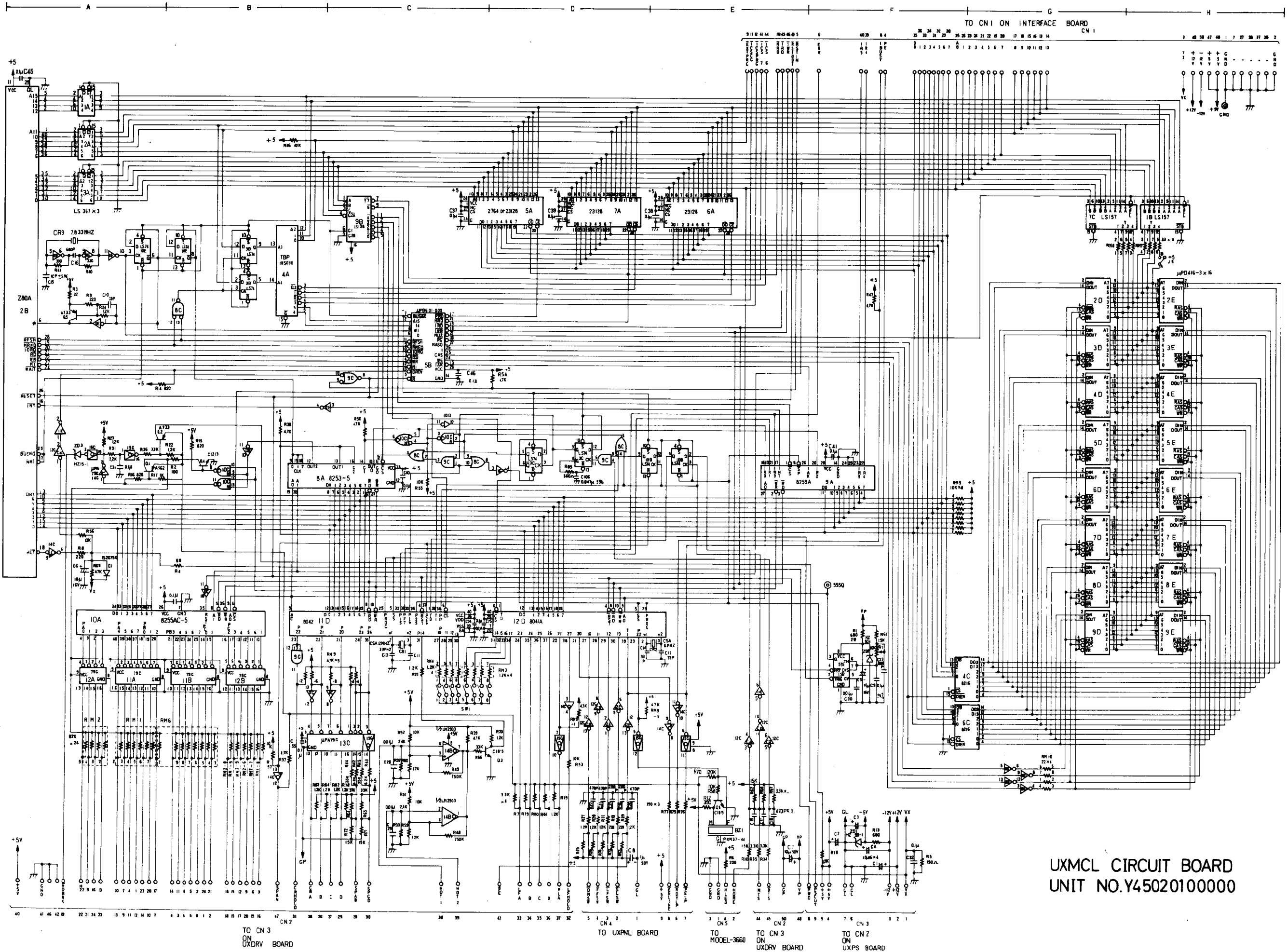
Lubrication and Adhesive Application Points Drawing A



Lubrication and Adhesive Application Points Drawing B



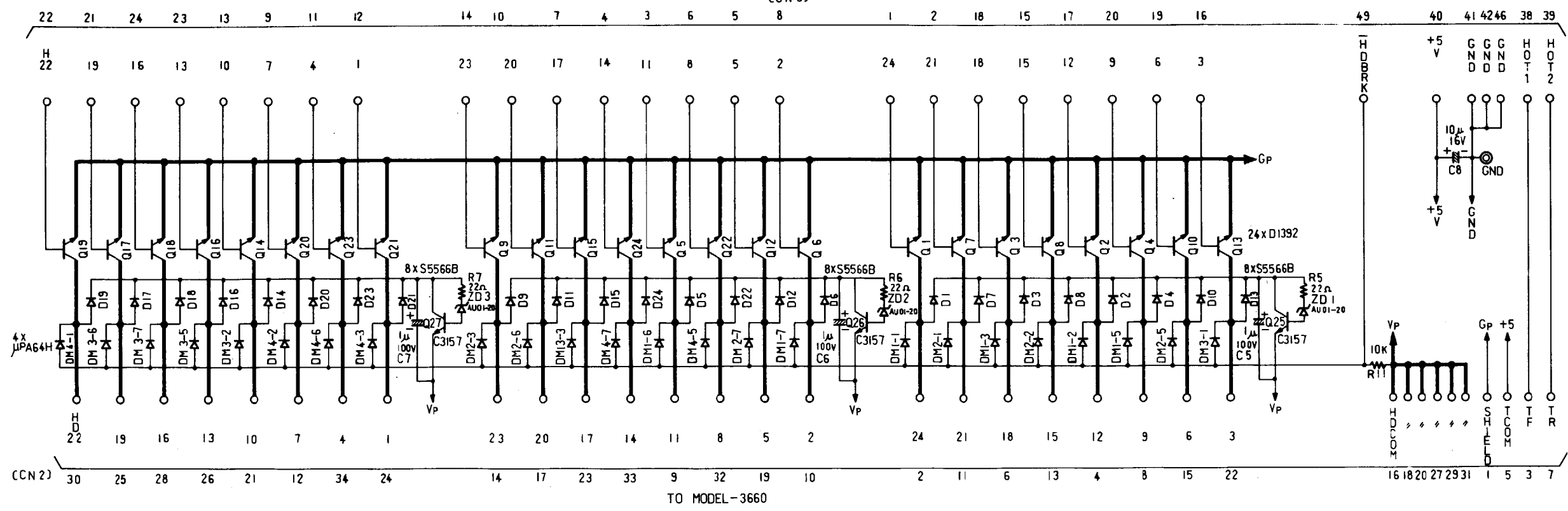
Lubrication and Adhesive Application Points Drawing C



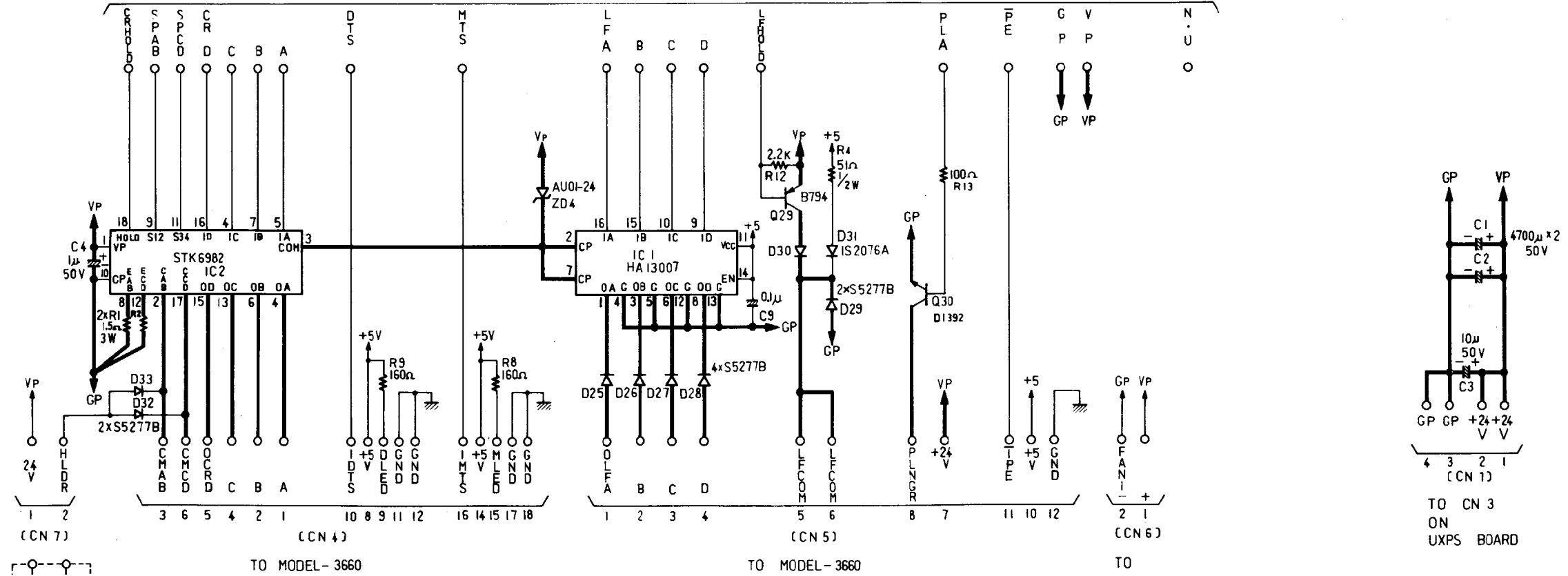
UXMCL CIRCUIT BOARD
UNIT NO. Y4502010000

A B C D E F G H

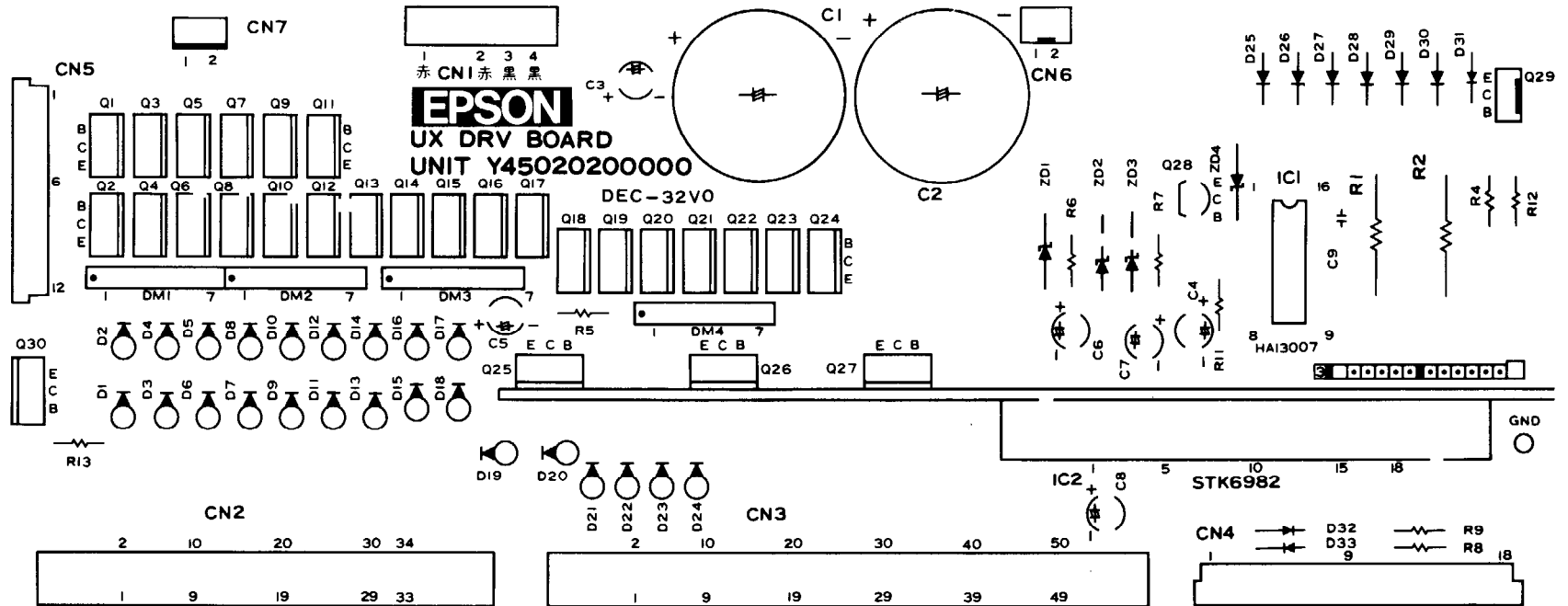
TO CN 2 ON UXMCL BOARD



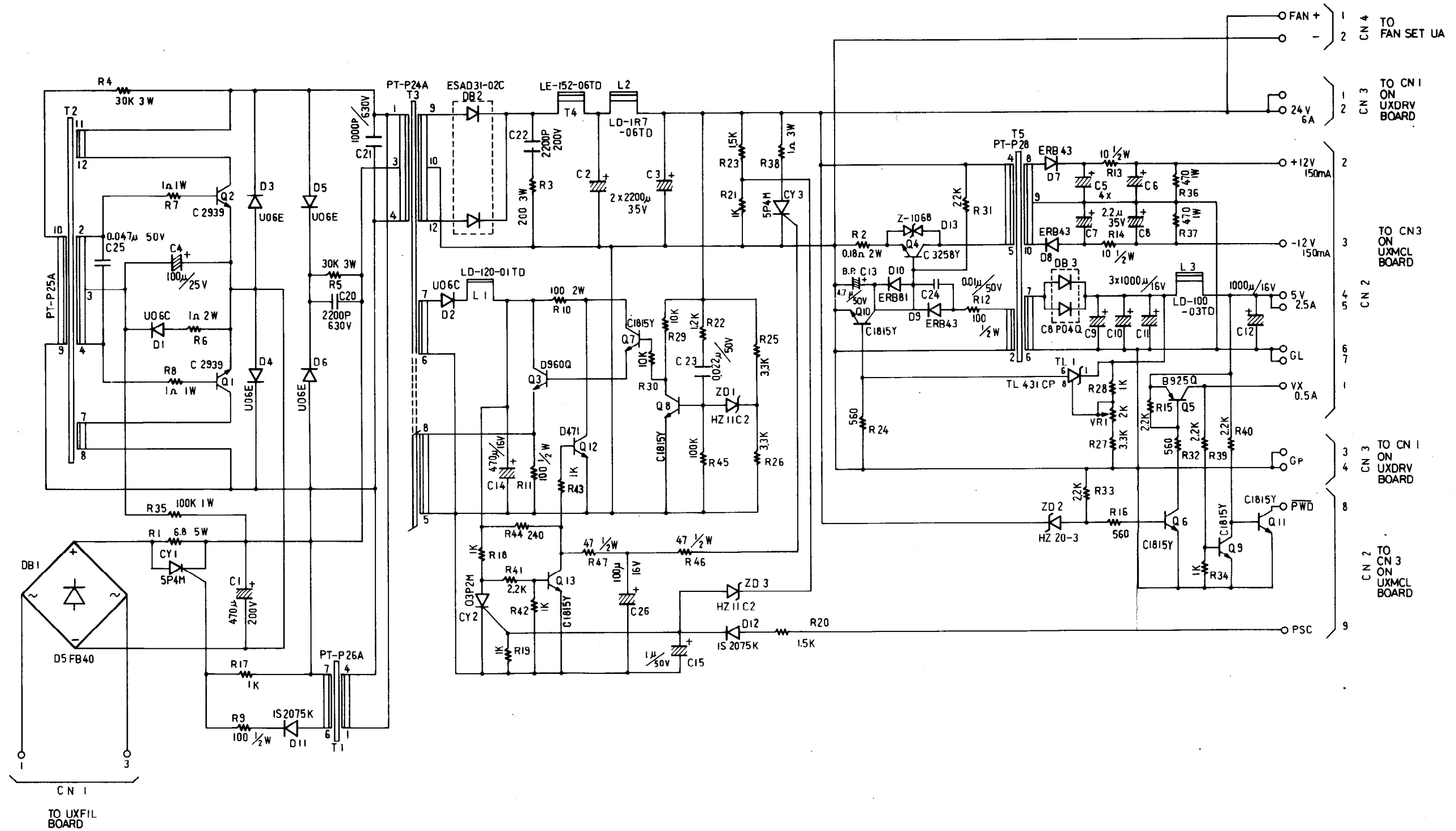
TO CN 2 ON UXMCL BOARD



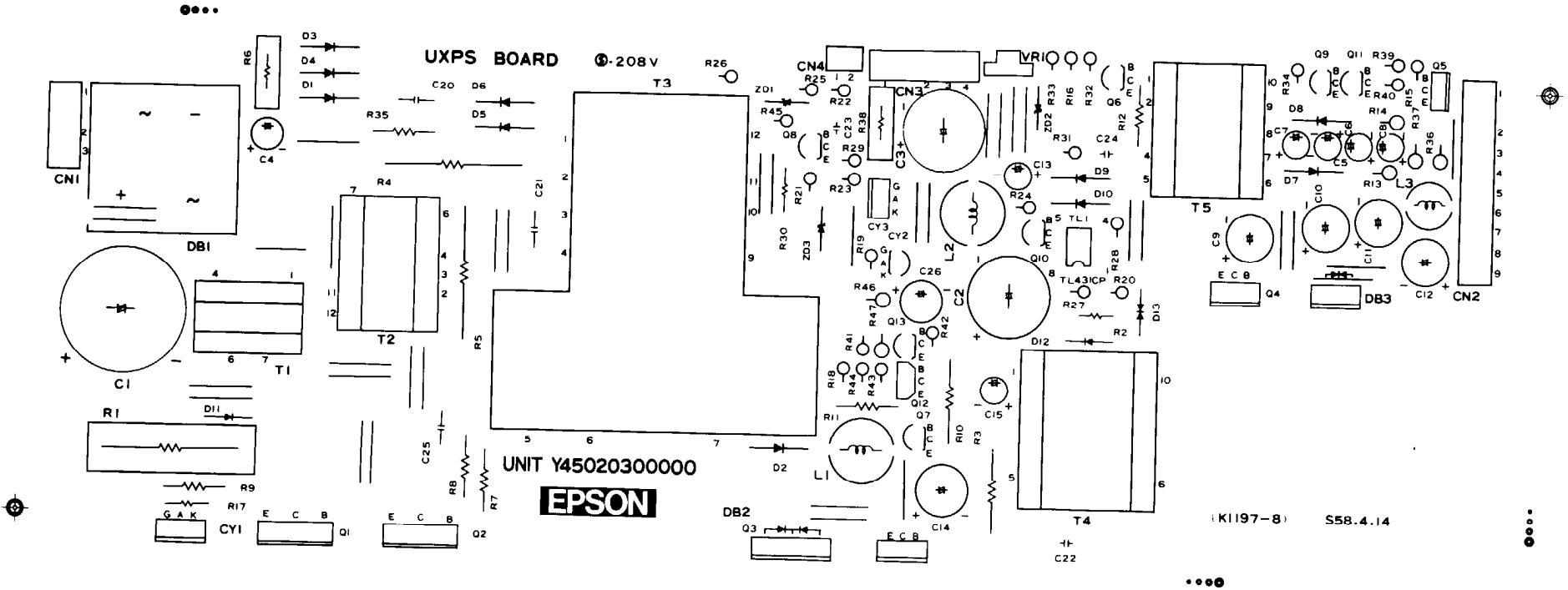
UXDRV CIRCUIT BOARD
UNIT NO. Y4502020000



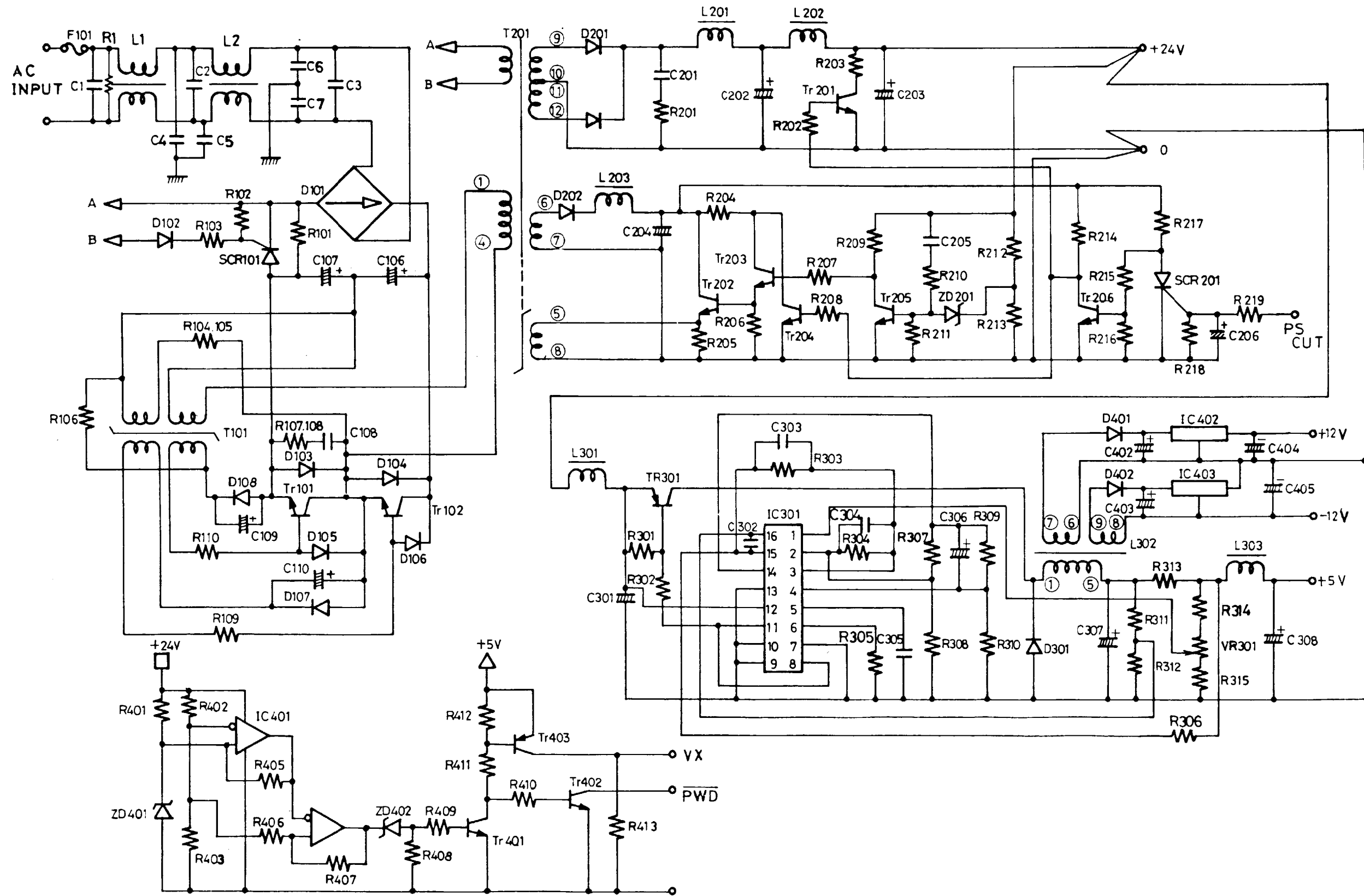
2
3
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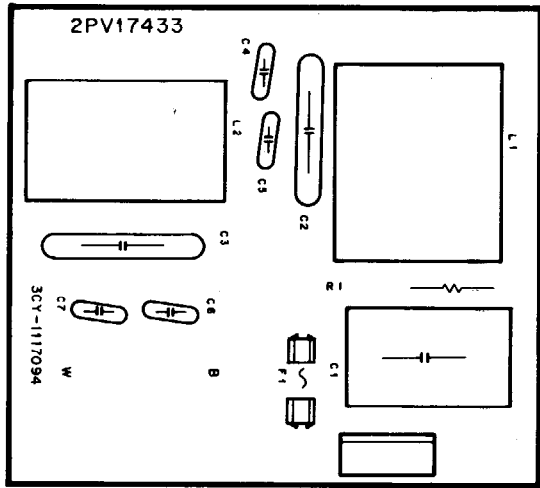
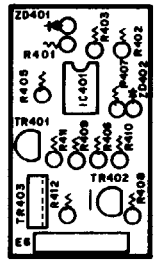
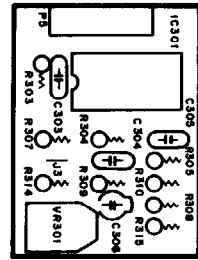
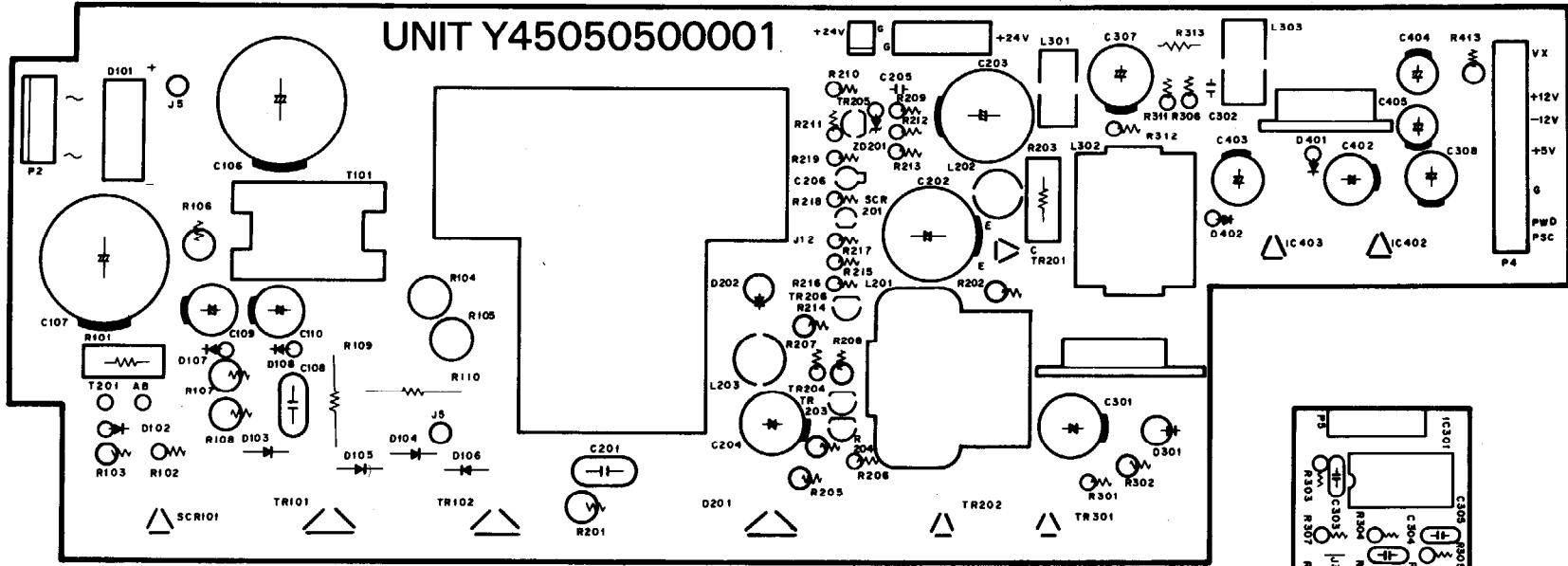
UXPS CIRCUIT BOARD
UNIT NO. Y45020300000



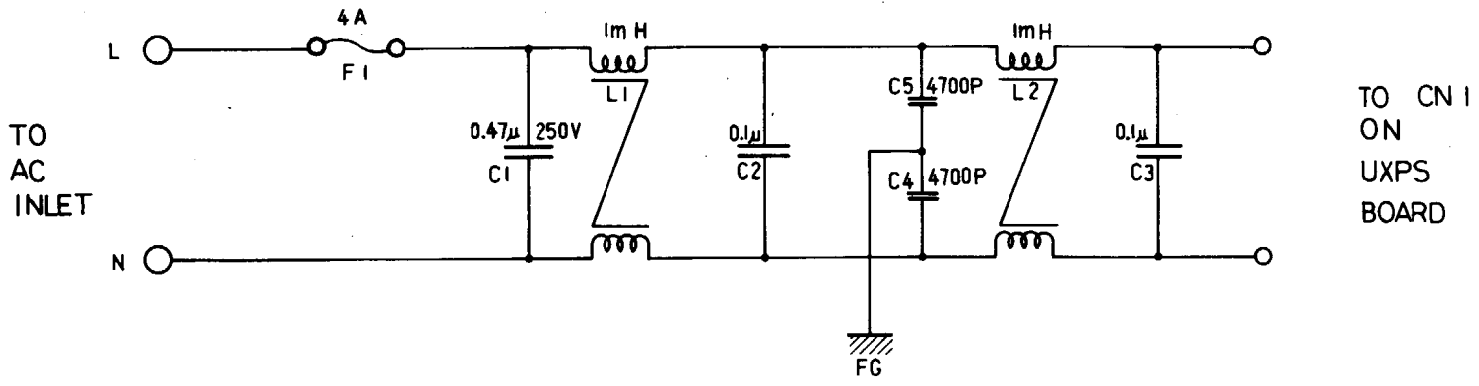
K1197-8) S58.4.14



PSU 24E CIRCUIT BOARD
UNIT NO. Y450505000



747



UXFIL CIRCUIT BOARD
UNIT NO. Y45020500000